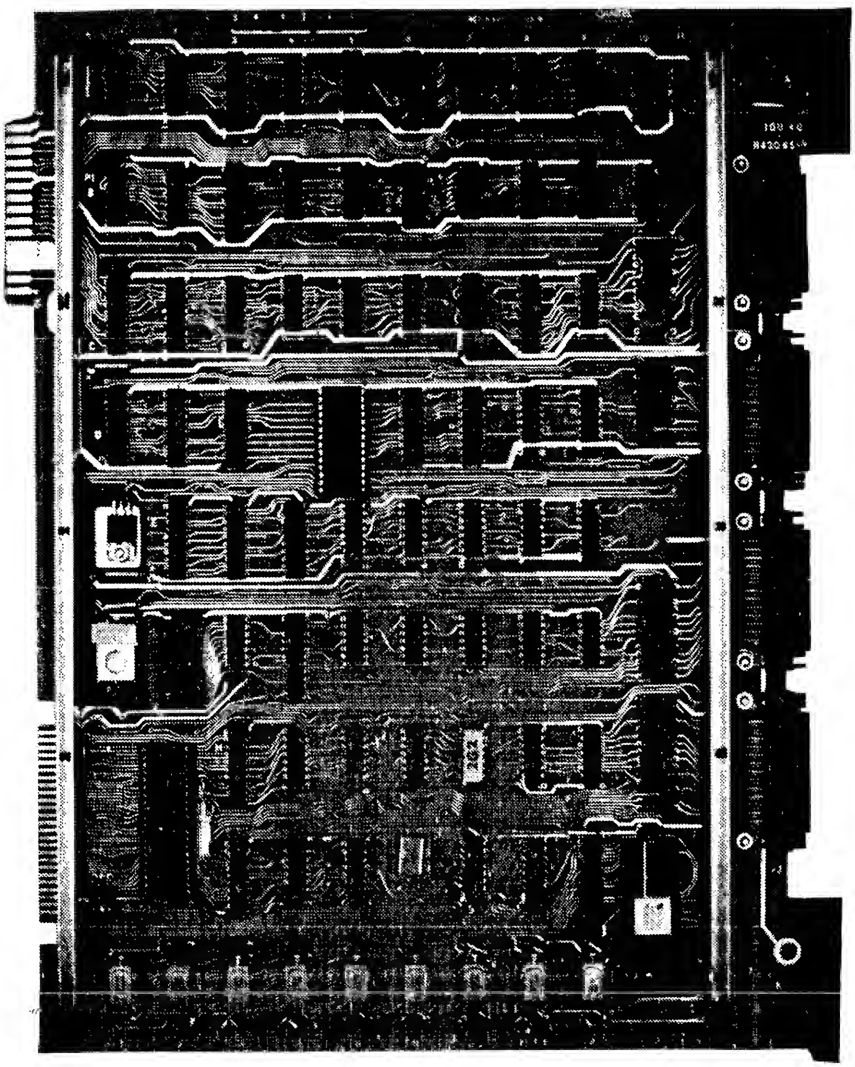
QANTEL
CORPORATION

IOU-40
Theory of Operation



M-4660

TD-4480

Technical Manual

IOU 40 Theory of Operation

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CAPSULE DESCRIPTION OF THE IOU-40

The IOU-40, a dual channel communications controller, was designed for interprocessor data exchange utilizing variable message syntax. Synchronous, asynchronous, and SDLC disciplines are included in this framework; each IOU-40 channel operates independently, interfacing a serial RS-232-C line.

Used in conjunction with the Qantel Device 40 board, each channel possesses automatic dialing capabilities and voice response functions.

The on-board Z-8Ø microprocessor is complemented by two Z-8Ø support IC's: the SIO, serial input-output, and the CTC, counter-timer circuit. Together, these IC's simplify and enhance the accomplishment of a wide variety of communication tasks.

A scheduler program contained in ROM acts to alternately service the two channels for smooth, simultaneous data transfer at speeds up to 9600 bits per second. Under certain conditions, a single active channel may be operated at a top speed of 19,200 bits per second.

A 16K dynamic RAM, accessible to the main CPU and the IOU-40's Z-8Ø, is used as a buffer during data exchange, as well as a storage area for programs downloaded from the CPU to control communication activities. Other locations within this RAM are used for variables applicable to current channel operations.

IOU 40's In Possible Configurations

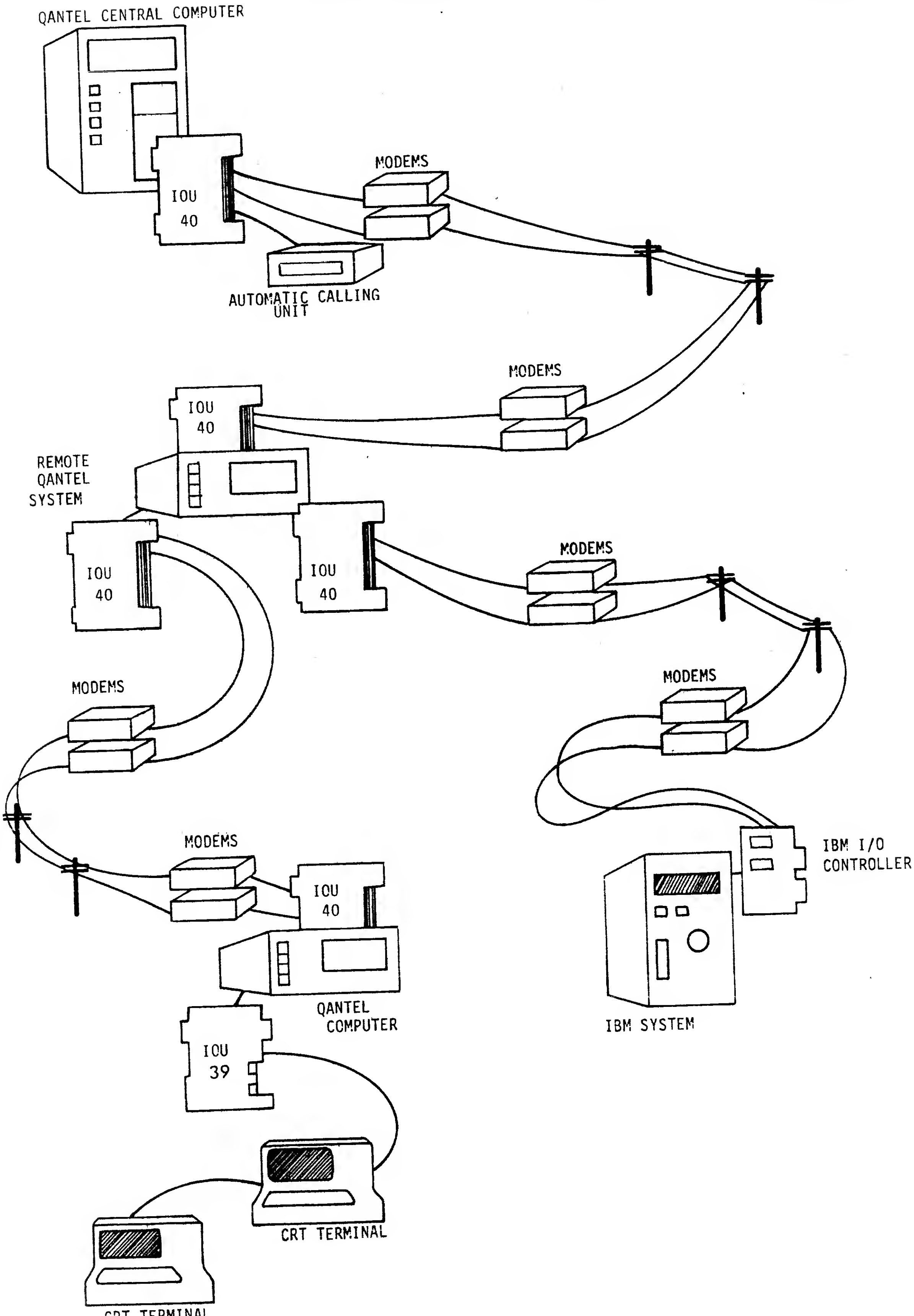


Figure 1

BLOCK DIAGRAM EXPLANATION

The basic elements of the IOU-40 and their interrelationships are illustrated in the block diagram. Control instructions from the CPU are sent out for decoding along the 4-bit IOE bus; data and other information passes through the bidirectional IOB bus.

The IOB bus is extended by a buffer for reduced loading to form the IOB-P1 bus. Through this bus, address values are loaded into the Address Counter, data is channeled into the Write register, and board-select addresses are routed to a comparator for CPU selection of the controller.

A decoded Write Control instruction from the CPU activates the load input of the low Address Counter, latching an address value supplied by the IOB bus at the arrival of STROBE. A subsequent Write Control instruction transfers the low Address Counter contents to the high Address Counter, and fills the low position with a new address value from the IOB bus. In this manner, the CPU can address the 16K Two-Port RAM.

The Two-Port RAM acts as a buffer during communication exchanges, as a storage area for variable status values, and as an area to accept programs downloaded by the CPU to match the IOU-40 to the necessary communication protocol.

Proper addressing of the RAM requires a row address (supplied by the low Address Counter) and a column address (from the high Address Counter), latched consecutively into the RAM memory chips through the A-bus. When the Z-8Ø wishes to address the RAM, it supplies a row address, followed by a column address by consecutively enabling first the low and then the high lines of its AD bus onto the A-bus.

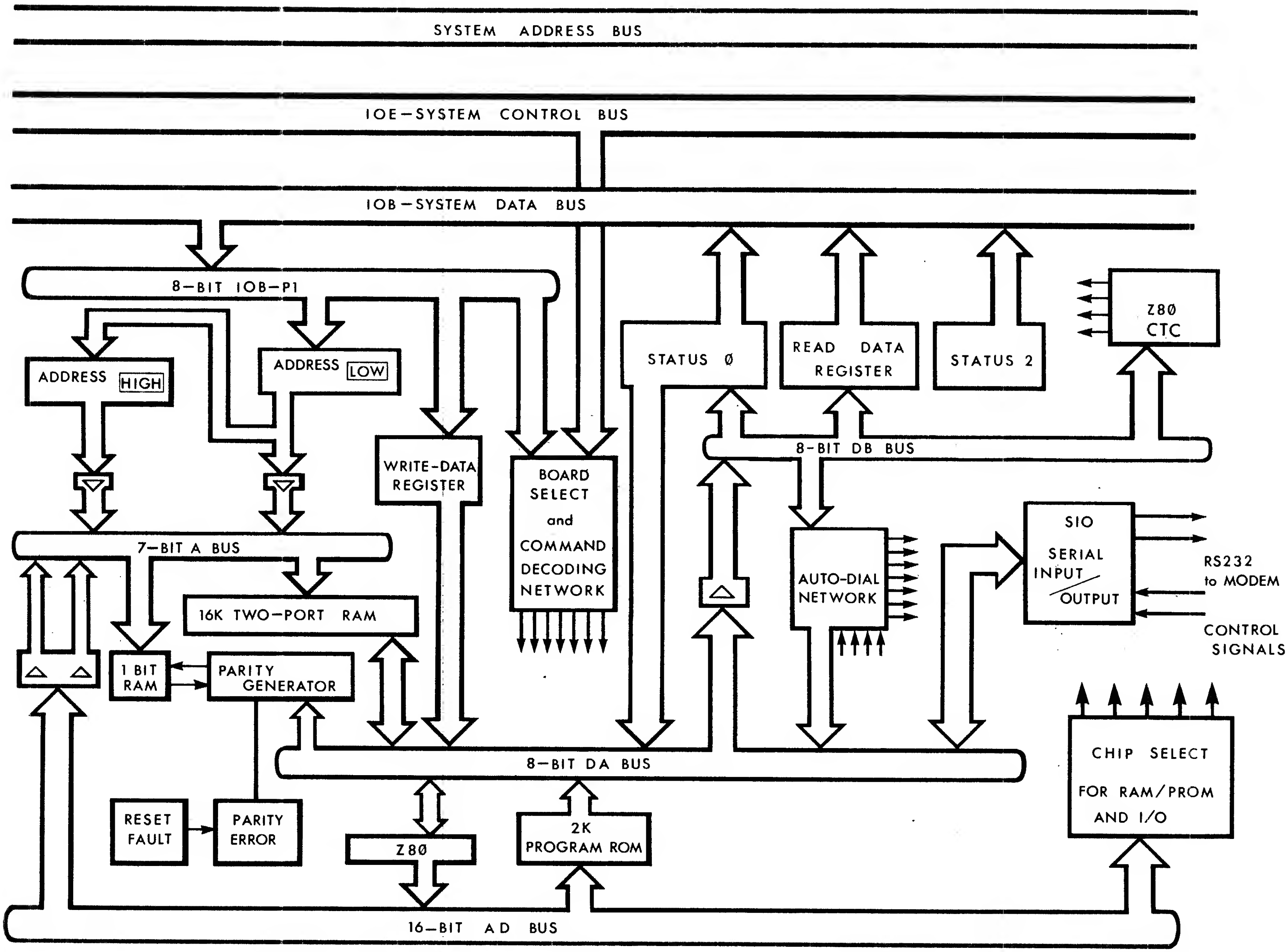


Figure 2

Overall Block Diagram for the IOU-40

BLOCK DIAGRAM EXPLANATION CONTINUED

The Parity Checking circuit produces an 'odd' or 'not odd' parity value for each data word passing into the RAM and stores it in a 16K by 1 RAM at an address location matching the address used for the Two-Port RAM. When the data is read out of the Two-Port RAM, the parity is again calculated and compared with the 'odd' or 'not odd' value stored in the Parity Memory. An error results in an indication sent to the Status Ø register and an error indicator triggering on the IOU-40 board.

The 2K ROM contains a scheduler which monitors the activities of Channel A and Channel B and allows them to function at a maximum data rate through a number of basic control sequences.

The Z-8Ø SIO is the site of data conversion. Besides basic parallel-to-serial conversion for transmitted data and serial-to-parallel for received data, the SIO is programmable for adaptation to a wide variety of serial data communications requirements. Synchronous, asynchronous, and SDLC protocols are handled over two independent channels; data integrity is internally monitored by various modes; and modem controls are handled.

Data routed to and from the CPU must pass through either the Read register or the Write register. By the CPU issuing a SET READ, Bus Request to the Z-80 is set. When the Z-8Ø issues a Bus Acknowledge, the Read register is loaded with the contents of the address location pointed to by the Address Counter. The Bus Request signal is then dropped (setting Service Request) and the CPU reads the data from the register (clearing Service Request and setting Bus Request). This process is repeated as often as necessary until terminated by the CPU.

When the CPU issues a SET WRITE, Service Request becomes active. After the CPU loads a data word into the Write register, Service Request is cleared and Bus Request is pulled. At the response of the Z-8Ø, the issuing of Bus Acknowledge, the word in this register is written into the memory location specified by the Address Counter (previously loaded by the CPU). When Bus Request drops inactive, Service Request is raised allowing the main CPU to continue the process.

The Status Ø register provides the CPU direct access to certain information (see Figure 12) concerning channel activity, data present in the RAM for reading, and Interrupt to the backplane. Although the Z-8Ø lacks the capability for reading the lower four bits of Status Ø (which are hardware flip-flops), it is able to read the upper four bits to determine if the CPU has responded to Interrupt. If so, the register will be cleared; this resetting occurs automatically whenever the CPU performs a READ STATUS 2.

By writing to the Status Ø register, the Z-8Ø accomplishes memory-mapped functions. The Parity Checking circuit can be enabled, the signal LOOP can be activated creating a Channel A feedback loop, and the Interrupt line to the backplane can be pulled by this means.

The Status 2 register consists of a tri-state buffer hardwired to a set value ($A3) to indicate to the CPU the controller's identity as an IOU-40.

The Z-8Ø CTC chip (Counter-Timer Circuit) controls the rate of data transmission and reception (this rate can also be controlled by external clock signals under certain circumstances), and acts as a running timer to ensure no longer than 10 milliseconds is allowed while waiting for a response from one

channel.

A Z-8Ø microprocessor drives, monitors, and regulates all on-board operations at a rate determined by the IOU-40's clock oscillator: 2.4576 MHz. Full test panel interface with the Z-8Ø is possible through the P2 connector.

The Auto-Dial Network is designed for use in conjunction with the Device 40, making it possible to automatically access telephone lines, receive incoming calls, record voice messages from the telephone lines, and respond by playing back prerecorded messages. The use of Auto-Call Units is also possible in order to handle telephone line interfacing.

The Chip Select is an octal decoder tied to the Z-8Ø's address lines used to generate memory-mapped signals for accessing ROM, Status Ø register, the Automatic Call-Up flip-flops, and for selecting internal or external Transmit Clocks, inputting status from the Auto-Dial Network, and writing to the Status Ø register for further memory-map operations.

EXPLANATION OF THE LOGIC DRAWINGS

The following section will discuss in page-by-page succession the Qantel Logic Drawings for the IOU-40 (included in the back of this manual). Copies of these documents including all updates and changes may be obtained by requesting Drawing No. D30720 from the Drafting Department.

Sheet 1 -- Low Status Zero

The proper addressing of the dynamic 16K RAM (eight RAM7 chips) requires the periodic output of a row address followed by a column address which acts as a strobe to latch the entire address value into the memory chips. When the CPU is providing the address to this RAM, the low 7 bits from the Address Counter provide the row address; the high 7 bits, the column address. The Z-8Ø supplies row and column address by sending out the proper values on its AD bus which are then multiplexed to the memory chips. The signals which create the necessary timing for accessing RAM are shown in columns 6,7, and 8 of sheet 1.

ADDRESSING THE TWO-PORT RAM -- ROW ADDRESS

Figures 3 and 4 illustrate the relative timing of the signals used during addressing operations. The CAD (Column Address) flip-flop produces the signals for determining which half of the Address Counter (or AD bus), high or low, will be used at a given time. CAD-ØP, the not-Q output, is driven high by MREQ-N or AD15-N going inactive which triggers the reset of the CAD flip-flop. CAD-ØP in combination with BUSAK-P will enable the buffers carrying the low order address information (in this case, the row address) to each of the memory chips. After a half clock cycle setup time, MREQ-N going low combined with the AD15-N signal low will produce RAS-N (Row Address Strobe), the signal to latch the 7 bits of row address information into the memory chips.

ADDRESSING THE TWO-PORT RAM -- COLUMN ADDRESS

To transfer the high order address information to the memory chips the CAD flip-flop must be set: RFSH-N going high applies a high to the 'D' input of the FF4 in conjunction with a positive-going clock edge to produce the 'set' condition. With the high order address information enabled through a buffer, the CAS (Column Address Strobe) flip-flop is triggered to 'set' (again, a half clock cycle is allowed for set-up time of the address value on the lines). This strobes the column address into the memory chips where internal multiplexing will generate the unique address location for READ or WRITE operations.

WRITE ENABLE

To enter data into the Two-Port RAM during a Write operation, an additional signal must be present besides the column and row address. Write Enable (WE-N) occurs when a particular set of conditions is satisfied: (1) RD-N is high (indicating a Read operation is not taking place). (2) RFSH-N is high. (3) MREQ-N and AD15-N are both low (active).

INCREMENTING THE ADDRESS COUNTER

A signal designated COUNT-N is applied to the Address Counter clock inputs automatically under the following conditions: (1) The main CPU is loading an address value. An untimed WRC signal provides a data input to a flip-flop that when clocked by a strobed WRC signal activates the load enables of the counters. (2) During a CPU read of data, RDD-N triggers COUNT-N. (3) The coincidence of the following signals produces COUNT-N: Service Request inactive (not-Q high); the CAS flip-flop set; BUSAK-P high; the Write Busy flip-flop high. These conditions occur

during a CPU write data operation. Note that cases '2' and '3' cause normal counting, while case '1' is a synchronous load operation.

STATUS Ø REGISTER -- LOW BITS TO THE CPU

A series of four Dual-D flip-flops buffered to the IOB bus lines 00 through 03 comprise the low half of the Status Ø register as seen by the main CPU. A READ STATUS Ø instruction sent on the IOE bus will enable these values plus the upper four bits which are firmware-controlled and loaded by the Z-8Ø. The upper four bits connect with the IOB bus lines 10 through 13. Figure 12 illustrates the bit designations as seen by the CPU. Figure 5 illustrates those signal combinations that alter the flip-flops in the Status Ø register.

Because of its unique nature, the Service Request flip-flop bears further consideration. Negative logic is used in this instance -- a high signal present at the not-Q output is an indication of a Service Request. The Q output is tied around to the Reset input so that in conditions where Set is applied (READ DATA or WRITE DATA commands from the CPU), Service Request cannot be activated. When Service Request is activated, the low output of Q locks the flip-flop in this state until another Set occurs to break lock.

BUS REQUEST

A Bus Request to the Z-8Ø is the result of one of two possible sequences:
(1) The CPU issues a SRD (SET READ) instruction, which sets the Read flip-flop and creates a high on one side of AND-gate 6C. The CPU then issues a RDD (READ DATA) which creates

a high out of the Q output of Service Request providing the other high to AND-gate 6C, producing BUSRQ-N.

The Z-8Ø will recognize a BUSRQ-N at the conclusion of its current machine cycle.

BUS ACKNOWLEDGE

Bus Acknowledge from the Z-8Ø acting in combination with other signals has a number of functions. BUSAK-N is gated through AND-gate 5E (if there is no Service Request and either the Read Busy flip-flop or the Write Busy flip-flop is active) to place a high signal at the data input of the Memory Request flip-flop. The next rising edge of the FASTCLK-P signal will set this flip-flop. The Q output high passes to Tri-state buffer 4E, already enabled by BUSAK-N being present, and the result is the signal MREQ-N being generated.

BUSAK-P in combination with the signal WR-1P (Q output of the Write Busy flip-flop) acts to enable the contents of the Write register onto the DA bus. The resultant actions of the CAD, CAS, RAS, and WE signals will direct the data on the DA bus into the correct Two-Port RAM location.

BUSAK-P is used in combination with the signals CAD-1P and CAD-ØP to provide row and column address multiplexing to the RAM chips. Tri-state buffers 3H and 3J (sheet 6) are enabled for Z-8Ø addressing; Tri-state buffers 3A and 3B for the CPU through the Address Counter.

SEQUENCE OF EVENTS IN A CPU READ OPERATION

(1) CPU loads the Address Counter to the desired location for the READ.

(2) CPU issues SET READ which turns on the Read Busy flip-flop in the Status Ø register.

(3) Bus Request goes true (the ANDed combination of Read Busy and no Service Request).

(4) When the Z-8Ø responds with Bus Acknowledge, the data word (accessed from the Two-Port RAM at the location indicated by the Address Counter) is transfered to the Read register.

CPU READ CYCLE TIMING

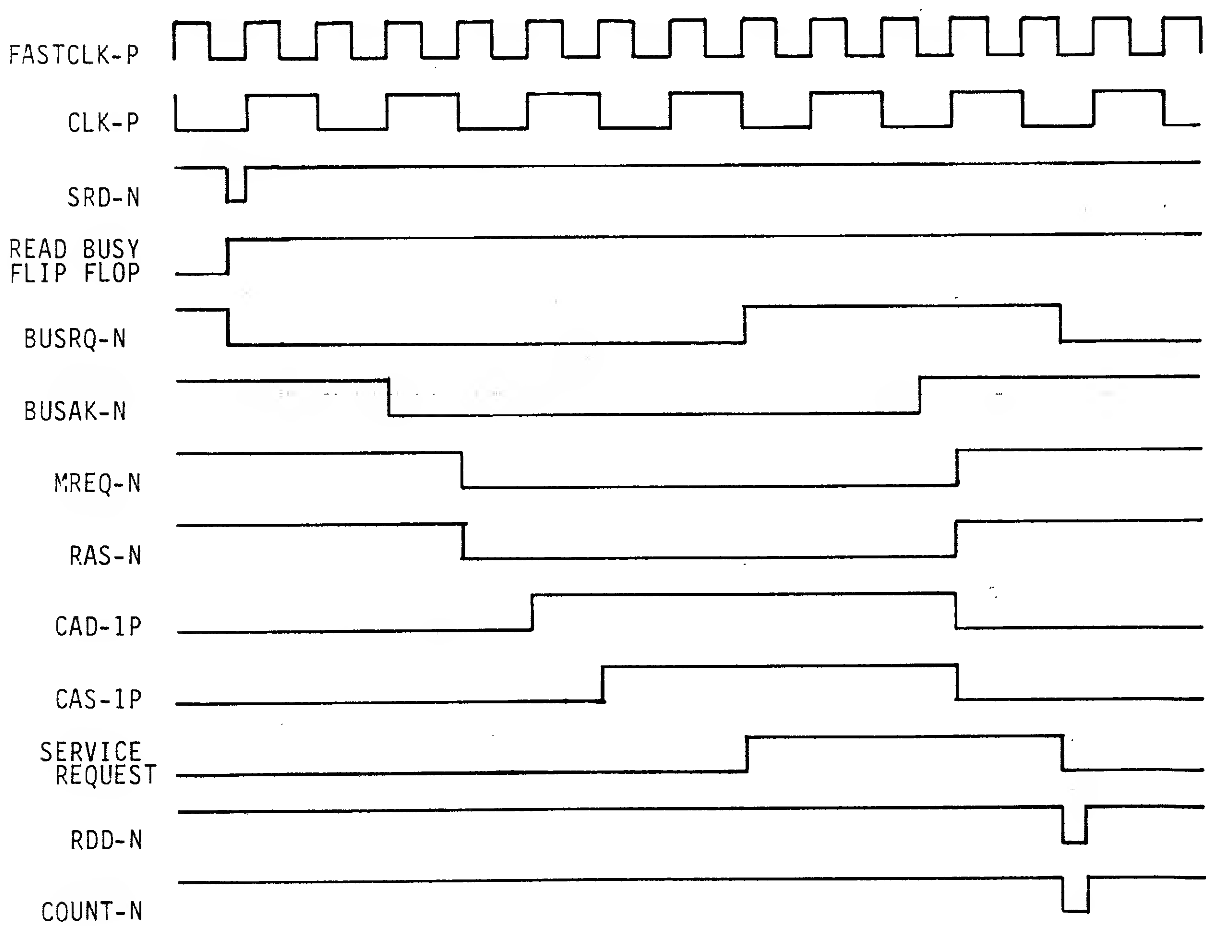


Figure 3

SEQUENCE OF EVENTS IN A CPU READ OPERATION CONTINUED

(5) This results in Service Request being set (thus dropping Bus Request).

(6) The CPU issues READ DATA (incrementing the Address Counter) to obtain the data word in the Read register. This turns off Service Request.

(7) Turning off Service Request raises Bus Request which starts the entire process over again.

(8) When the CPU has completed its Read operation, it issues TERMINATE, ending the sequence.

SEQUENCE OF EVENTS IN A CPU WRITE OPERATION

(1) CPU loads the Address Counter to the desired location for the WRITE.

(2) CPU issues SET WRITE which turns on the Write Busy flip-flop in the Status Ø register and sets the Service Request active.

(3) CPU issues WRITE DATA which loads the data word into the Write register, turns off Service Request, and raises Bus Request.

(4) When the Z-8Ø responds by issuing Bus Acknowledge, the value in the Address Counter is given to the Two-Port RAM.

(5) The contents of the Write register are written into the designated location in the Two-Port RAM.

(6) Service Request is raised, Bus Request is dropped, and the Address Counter is incremented.

(7) This process continues until the CPU issues TERMINATE.

CPU WRITE CYCLE TIMING

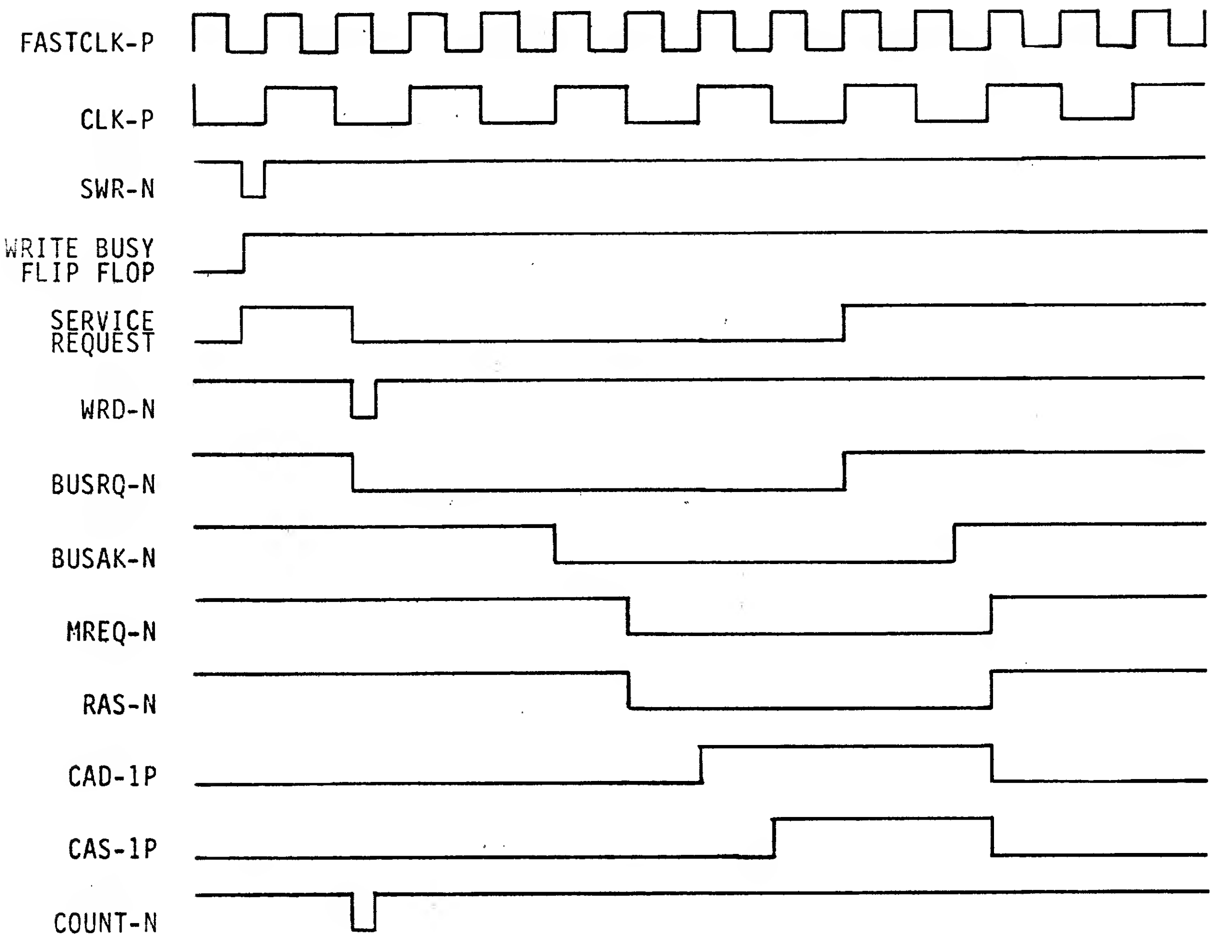


Figure 4

LOW STATUS 0 TO CPU

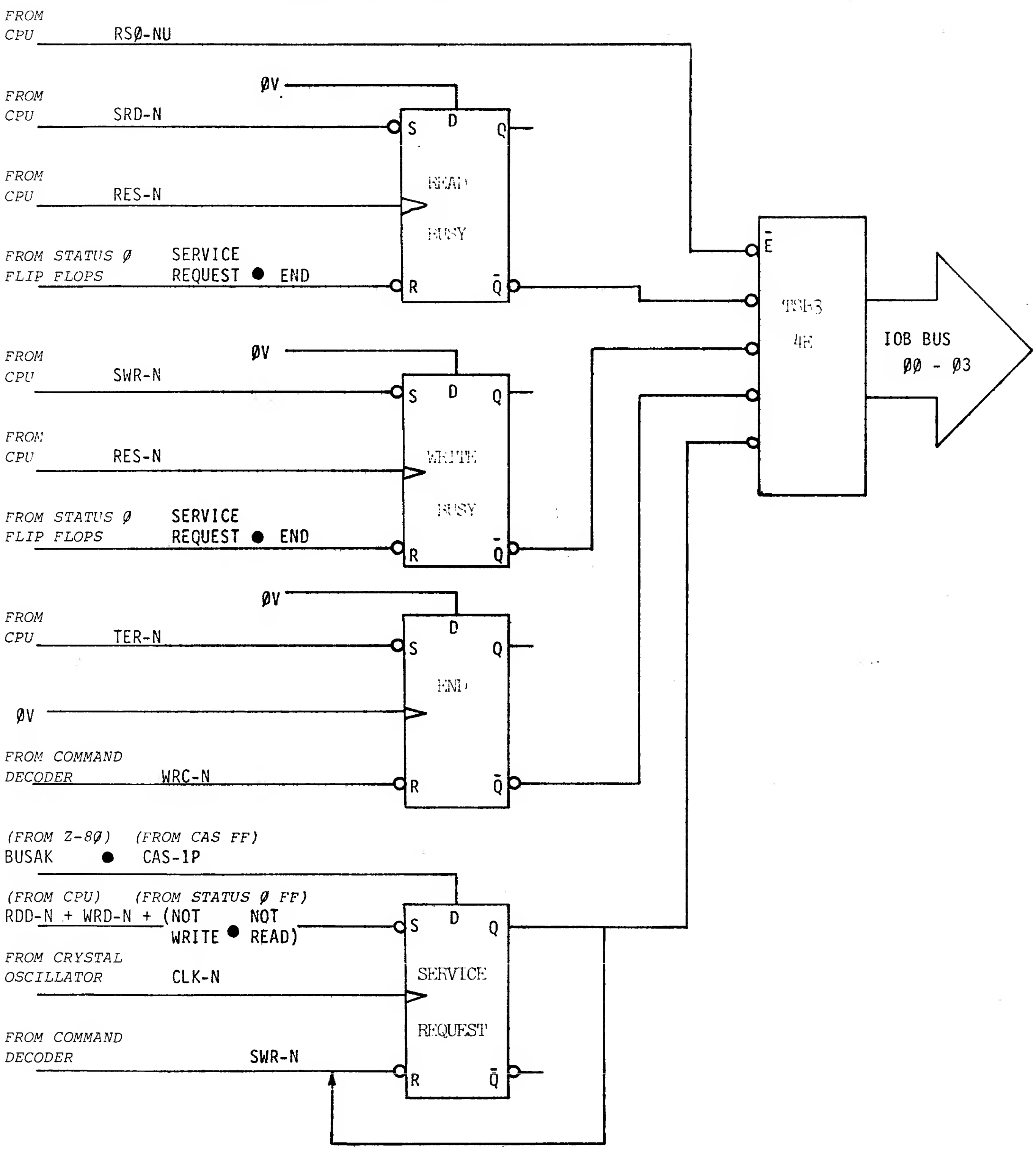


Figure 5

EXPLANATION OF THE LOGIC DRAWINGS

Sheet 2 -- Address Counter

Physically, the Address Counter consists of four 4-bit Synchronous Counter chips, 74LS161's. They are loaded exclusively by the main CPU by issuing two consecutive WRITE CONTROL commands, the 'control word' (sent out on the IOB bus) representing the high or low order values of a 14-bit address. The first WRITE CONTROL instruction parallel loads the lower counters with the value on the IOB bus (LOAD-N activates the load pins; COUNT-N, originating on sheet 1 of the logics provides the clock). The second WRITE CONTROL instruction loads the low order address value into the high order position, and loads the actual low order bits into the low order position.

The address is introduced to the Two-Port RAM memory chips along the 7-bit A-bus through Tri-state buffers 3A and 3B in two separate steps. The coincidence of the signals CAD-1P and BUSAK-P enables the high order address onto the A-bus, representing the column address. CAD-ØP and BUSAK-P enables the low address value onto the A-bus, representing the row address.

The signal RES-N from the CPU will clear the Address Counter.

EXPLANATION OF THE LOGIC DRAWINGS

Sheet 3 -- Data Register

The Write register and the Read register act as intermediary storage locations between the main CPU and the IOU-40 for data transfer. Each is loaded with a data byte by the appearance of a clock signal and read (through internal tri-state buffering) by the appearance of an enable signal.

The Write register is loaded with a data word from the IOB-P1 bus at the arrival of WRD (Write Data) at the clock input. The Z-8Ø enables the internal tri-state buffer by issuing BUSAK-P. BUSAK-P and WR-1P, the output of the WRITE BUSY flip-flop, combine to produce the enable signal which then allows the data byte to be accepted off the DA bus into the memory location predetermined by the memory address gating.

The Read register is loaded by the trailing edge of the BUSRQ-N signal. The CPU selects the location in the Two-Port RAM it wishes to READ by loading a value into the Address Counter. Cued to the completion of the register loading by Service Request coming active, the CPU enables the data byte onto its IOB bus by issuing RDD-NU (READ DATA).

Tri-state buffers 1C and 2D are held constantly active by low inputs to their enable pins.

EXPLANATION OF THE LOGIC DRAWINGS

Sheet 4 -- 16K Byte Dynamic RAM

The 16K by 8 bit Two-Port RAM consists of eight 16K by 1 dynamic memory chips. Addressing takes place on the 7-bit A-bus; the CPU initiates addressing through the Address Counter; whereas, the Z-8Ø uses the AD bus.

The total address is introduced to the memory chips in two separate stages: a 7-bit row address (latched into the chip with the RAS-N signal) followed by a 7-bit column address (the signal CAS-ØP acts as a control for outputting data). The signal WE-N is activated to write data into the Two-Port RAM.

During Refresh cycles only the RAS-N signal is applied to the memory chips. Each Refresh cycle, automatically initiated by the Z-8Ø, will refresh one of the 128 row address locations. All 128 row addresses must be refreshed every 2 milliseconds or less.

Data is outputted and received by the Two-Port RAM on the DA bus.

EXPLANATION OF THE LOGIC DRAWINGS

Sheet 5 -- Z-8Ø Status and ROM

The Status Ø register exists for the Z-8Ø in a different context than it does for the CPU. The lower four bits of Status Ø (as seen on sheet 1 of the logics) are entirely hardware controlled. These bits are read only by the CPU and cannot be accessed by the Z-8Ø.

The high Status Ø register, as represented by half of the octal flip-flop 3D, provides the CPU with four more bits of information to be coupled onto the upper four lines of its IOB bus. The Z-8Ø provides the information for the high Status Ø by writing the pseudo-memory location $0800. This generates the signal SOH-N (decoding takes place on sheet 6 by the octal decoder 4H) which provides a clock for latching the data on the DB bus (provided by the Z-8Ø on the DA bus).

The other half of the octal flip-flop provides the Z-8Ø with the ability to activate two control signals (by writing binary 1's into the proper positions): PEN-P and LOOP-P. PEN-P is the Parity Enable signal for initializing the Parity Checking circuit. LOOP-P creates a feedback loop in Channel A by enabling a buffer.

The bit designations as written to this register by the Z-8Ø are:

2**0.........Set Loop Test Mode
2**1.........Enable Parity Circuit
2**2.........Not Used
2**3.........Interrupt
2**4.........Flag 1
2**5.........Channel A Terminate
2**6.........Channel B Terminate
2**7.........Inoperative

EXPLANATION OF THE LOGIC DRAWINGS CONTINUED

The Status 2 register is hardwired to a value ($A3) to indicate to the CPU the IOU-40's identity. The act of the CPU reading the Status 2 register clears the high Status Ø register (this departs from conventional backplane protocol). RS2-NS ties directly to the Status Ø FF5 reset pin.

The IOU-40 can detect the clearing of the Status Ø register by reading pseudo-location $1C00. The memory-mapped signal output generated by performing a Read to this address enables the Tri-state buffer 3E coupling the high four lines from the Status Ø register to the DA bus. The signal is known as SOI-N, Status Ø In.

Two RPROM2 chips, each 1K by 8, contain the Scheduler program. The logical handling of Channel A and B activities to ensure efficient data transfers is the responsibility of the Scheduler program. Addressing of this memory takes place on the address lines ADØØ through ADØ9. AD1Ø and AD11 are decoded (see the octal decoder 4H on sheet 6) to produce the chip select signals ROMØ and ROM1. Data is released onto the DA bus.

Columns 2 and 3 of this sheet illustrate the power supply filtering and voltage regulation for the memory chips.

EXPLANATION OF THE LOGIC DRAWINGS

Sheet 6 -- Z-8Ø

The crystal oscillator (seen on the lefthand portion of the sheet) produces a 4.9152 MHz square-wave which is divided in half by the flip-flop 4J for a clock signal to the Z-8Ø of 2.4576 MHz. Other timing signals originating from this source and their functions include:

> FASTCLK-P -- 4.9152 MHz -- (extended to Sheet 1).... Clock input to the MEMRQ flip-flop.
>
> CLK-P -- 2.4576 MHz -- (extended to Sheet 1 and 8).... Clock input to the CAD flip-flop enabling the column address to the Two-Port RAM. Clock to the RIO Timing counter.
>
> CLK-N -- 2.4576 MHz -- (extended to Sheet 1)....Clock input to CAS flip-flop which strobes the RAM chips after the address is stable.

The Z-8Ø's control, address, and data lines are all available for test purposes via the P2 connector. Note that the octal decoder 4H tied to address lines AD15, AD12, AD11, AD1Ø, MEMRQ-N, and RFSH-N provides control functions for the board through memory-mapping:

Memory-Mapped Address	Signal and Function
$0000.....	ROMØ-N -- Selects the chip representing the lower half of the Program ROM.
$0400.....	ROM1-N -- Selects the chip representing the upper half of the Program ROM.
$0800.....	SOH-N (Status Ø High) -- Clocks data on the DB bus into the Status Ø register.
$0C00.....	SCLK-N (Select Clock) -- Acts to select internal or external Transmit Clocks by clocking the data inputs of flip-flop 1ØB. A

high on DBØ when clocked selects internal Transmit Clocking for Channel A; a high on DB1, internal Transmit Clocking for Channel B.

$1000.....ACUA-N (Automatic Call-Up Channel A) -- Routes control signals to Dialer Network by clocking data into flip-flop 7D.

$1400.....ACUB-N (Automatic Call-Up Channel B) -- Routes control signals to Dialer Network by clocking data into flip-flop 6D.

$1800.....TACU-N (Channel A/B Dialer Status) -- Inputs status information from the dialing network.

$1C00.....SOI-N (Status Ø In) -- Inputs the high bits of the Status Ø register for examination.

Address line 15, AD15-N, combined with MREQ-N provide access to the Two-Port RAM (see Sheet 1, Column 7). AD15-N when not actually activated by the Z-8Ø (as the inversion of AD15-P) will be active when the Z-8Ø is in a 'tri-state condition' (such as occurs when the Z-8Ø issues BUSAK) due to a pull-up resistor on the input as seen at the top of Column 6. This feature allows the CPU access to the Two-Port RAM when the Z-8Ø is not handling the bus lines.

A complete description of the Z-8Ø inputs and outputs is provided by the *ZILOG DATA BOOK (Zilog, Inc.; 10340 Bubb Road, Cupertino, California, 95014).*

As seen in Columns 1, 2, and 3, the Z-8Ø may directly address the Two-Port RAM along the A-bus by multiplexing of the AD lines ADØØ through AD13. ADØØ through ADØ6 produce the row address and ADØ7 through AD13 produce the column address through the

enabling of Tri-state buffers 3J and 3H. CAD1P and CADØP supply the high and low enables to these buffers whenever BUSAK-N is absent.

EXPLANATION OF THE LOGIC DRAWINGS
Sheet 7 -- Select and Command Decoding

The process of selecting the controller for a CPU operation requires two necessary components. The COM3 chip 4A compares the value entered on the address switches (physically set on the IOU-40 board) with the value present on the lower lines of the IOB bus. If the two inputs are equal, the comparator output from pin 6 supplies a high to the 'D' input of the Select flip-flop. This high will be clocked into the Select flip-flop if an $F is present on the IOE bus in coincidence with a STROBE from the main CPU. The not Q output from the Select flip-flop will then supply one enable to the octal decoder pair 7A and 8A.

Octal Decoder 7A decodes those commands from the main CPU that are strobed commands (synchronized by a timing pulse). The strobed commands consist of the following values on the IOE bus:

Hex value	Microinstruction
\$0................	RDD-N
\$2................	WRD-N
\$3................	WRC-N
\$4................	RIO-N
\$5................	SRD-N
\$6................	SWR-N
\$7................	TER-N

Anything above a $7 will place a high on IOE3, which disables the octal decoder 7A by forcing a high to pin 4 which requires a low for enabling.

Octal decoder 8A decodes those microinstructions for which the strobe signal is unnecessary: RS2-NU; WRC-NU; RSØ-NU; RDD-NU.

An additional signal -- RS2-NS -- is the product of STROBE and RS2-NU routed through an AND gate. RS2-NS resets the Status Ø register.

Column 3 illustrates the gating network that combines RD-N and IORQ-N to produce IORD-P; and WR-N and IORQ-N to produce IOWR-P. IORD-P and IOWR-P are used for test purposes only.

Columns 1 and 2 illustrate the development of the Transmit Clocks for Channels A and B. If the Z-8Ø places a high on DB-1, at the rising edge of SCLK-N the flip-flop will be set, outputting a high from pin 5. This high allows the clock signal CLKB-P to pass through AND gate 8D. It is then directed to the Z-8Ø SIO Transmit Clock input for Channel B. A similar situation exists for Channel A clocking except that the select occurs with a high on DBØ.

Otherwise, if not deliberately selected, the Transmit Clocks originate from the modems via DBB and DBA.

EXPLANATION OF THE LOGIC DRAWINGS

Sheet 8 -- SIO and Speed Select; Internal Clocks

The Z-8Ø SIO (Serial Input, Output) on this sheet is capable of a wide variety of communication tasks through the direction of the Z-8Ø microprocessor. Selecting a control function by raising a high signal on ADØ4-P designates that the incoming data on DAØ-P through DA7-P should be interpreted by the SIO as a command for the channel selected by ADØ5-P (high for B, low for A). The nature of this control information determines such variables as communication protocol (synchronous, asynchronous, or SDLC) and other elements of the selected message syntax. Details of the operation of the SIO can be obtained from the *ZILOG DATA BOOK*.

Each channel has an individual transmit register and receive register and uses incoming clock signals to regulate serial-to-parallel conversion and parallel-to-serial conversion. These incoming clock signals may originate either from a modem or from the Z-8Ø CTC depending on the Z-8Ø microprocessor selecting the appropriate mode of operation. The gating for the selection of the receive clocks is shown on sheet 9; the transmitter clocks, sheet 7.

Outputs of the SIO to the modem include:

TxDA.....Transmitted Data, Channel A
TxDB.....Transmitted Data, Channel B
RtSA.....Request to Send, Channel A
RtSB.....Request to Send, Channel B

The row of op-amps directly below the SIO serves to convert TTL signal levels to RS-232-C standards.

The Tri-state buffer 8C normally routes incoming signals from the modem lines to SIO inputs. Inputs are:

EXPLANATION OF THE LOGIC DRAWINGS CONTINUED

RxDA.....Received Data, Channel A

RxDB.....Received Data, Channel B

CtSA.....Clear to Send, Channel A

ACRA.....Data Set Ready, Channel A

The conversion of these incoming modem signals from RS-232-C levels to TTL takes place on sheet 10, columns 7 and 8. Notice that these signals are routed through the tri-state buffer only when LOOP-P is present, indicating that the Loop-back Test Mode is not taking place. The LOOP-N signal ties the Channel A Request to Send and Clear to Send lines together and feeds the Transmitted Data output into the Received Data input. Data Set Ready is simulated by the incoming signal CD-P off the DB7 line.

Channel B's Clear to Send and Data Set Ready inputs are shown arriving unbuffered from the modem.

RIO TIMING

The 4-bit synchronous counter near the center of the page responds to a System Reset or RESET I/O Device Control by loading four Ø's into the counter. At this time the output at pin 15, carry, will be low which enables the chip for counting and supplies a low reset pulse to the SIO, CTC, Z-8Ø, and the Transmit Clock Select network. The reset will be held until the counter reaches 15 -- the carry output going high disables the count and forces a high to all the previously mentioned reset inputs, ending the reset process. This high will be maintained until RES-N is brought active (either from System Reset or RESET I/O, repeating the entire action. This sequence assures a sufficient number of clock cycles take place for a full reset of the Z-8Ø, CTC, and SIO.

Z-8Ø CTC

The CTC chip (Counter-Timer Circuit) at the right-hand portion of the page is programmed by the Z-8Ø to generate the correct baud rate for each channel. ZC1's output at pin 8 is divided in half by flip-flop 5B to produce the CLKB-P signal, which is used as the basis for Channel B's Transmit Clock and Receive Clock. ZCØ's output at pin 7 produces a pulse at its programmed interval and in similar fashion generates CLKA-P, the Transmit and Receive Clock source for Channel A (when not derived from the modem).

The CTC is programmed by the Z-8Ø microprocessor so that at regular intervals an output is generated from pin 9, ZC2 to trigger a timer circuit at pin 20, TC3. The timer is set up to produce an interrupt (outputted from pin 12) to the Z-8Ø at 10 millisecond intervals to prevent lags in channel response times any greater than that period.

EXPLANATION OF THE LOGIC DRAWINGS

Sheet 9 -- Dialers

The Auto-Dial Network provides a direct method for either channel to access telephone lines or receive incoming calls. The flip-flops 7D and 6D hold information routed down the DB bus, latched by the clock signal ACUA-N or ACUB-N (Automatic Call-Up A or B). This information corresponds with signals, converted to RS-232-C levels by the string of OP amps, given the following meanings:

ACRQ / BCRQ......Call Request
ADPR / BDPR......Data Present Strobe
ANB1 / BNB1
ANB2 / BNB2
ANB4 / BNB4
ANB8 / BNB8......Binary-weighted lines for conversion to telephone tones

These signals are linked to either the Device 40 or an Auto-Call Unit where digital-to-analog conversion takes place. Incoming signals carrying status information about the telephone connections are available by enabling a Tri-state buffer, 9J, and are designated as follows:

ADLO / BDLO......Data Line Occupied
ADSS / BDSS......Data Set Status
AACR / BACR......Abandon Call and Retry
APND / BPND......Present Next Digit

Within columns 5 and 8 of this sheet, the gating networks for the Receive Clock for Channels A and B can be seen. The Receive Clock signal is applied directly to the respective Receive Clock pin of the SIO and is selected as to internal or external origin depending on the value on line DB6 entered into the Auto-Call flip-flop. A high out of pin 2 of the Channel A Auto-Call flip-flop will allow the Receive Clock from the modem to pass

through AND gate 9D. A low out of pin 2 allows the CLKA-P signal to pass through this AND gate. This method is duplicated for the selection of the Channel B Receive Clock.

EXPLANATION OF THE LOGIC DRAWINGS
Sheet 10 -- Parity Logic

During the initialization process, the Scheduler program takes the data from each location in the Two-Port RAM and writes it back into the RAM. This operation ensures the recording of a parity value in the Parity RAM matching whatever spurious data was contained in the Two-Port RAM at turn-on.

As data is being written into the Two-Port RAM, the PGC2 chip, the Parity Generator, receives the same data on the DA bus and outputs a binary one if the parity is odd. This value is gated through the Tri-state buffer 4F which is enabled by the WE-N signal (Write Enable) and then stored in the Parity RAM at a location which has just been multiplexed through the A bus.

When data is read out of the Two-Port RAM, the Parity RAM expels an 'odd' or 'not odd' value corresponding with the accessed data. This parity value is routed back through the same Tri-state buffer (by CAS-ØP active and WE-N inactive enabling the correct half of the buffer). The Parity Generator checks the byte from the Two-Port RAM currently on the DA bus, computes parity, and then the incoming recorded parity value received at pin 1 will cause the Parity Generator to output a Ø if the previously calculated parity agrees with the currently calculated value. This Ø routed through the buffer to the 'D' input of the flip-flop 5H will not activate the PER-P (Parity Error) line; whereas, a '1' results in the flip-flop setting at the first rising clock edge and the Parity Error is noted in the Status Ø register. A '1', of course, occurs if the calculated Parity Generator value does not agree with the stored parity value.

Additionally, the Parity Error flip-flop causes the triggering

of an error indicator, physically present on the IOU-40 board.

The signal RES-N resets the upper portion of the flip-flop 5H, forcing a low out of the Q output at pin 9. This low will hold the lower portion of the flip-flop 5H (the Parity Error flip-flop) in a reset condition making it unresponsive to changes. Parity is enabled by activating the signal PEN-P. Its rising edge acts as the clock to input the tied-high data line (pin 12) of the upper portion of flip-flop 5H, setting it. This removes the reset from the Parity Error flip-flop and subsequent highs to its input accompanied by a clock signal will result in the PER-P signal being driven high.

Columns 3 & 4 illustrate those gates remaining unused on the IOU-40.

EXPLANATION OF THE LOGIC DRAWINGS
Sheet 11 -- Block Diagram and Connectors

The final page of the logic drawings illustrates the pin-out designations for the six connectors: P1 through P6. A block diagram provides a reference to the relationships of the various components to the bus lines for an overall view of the controller's operation.

IC'S USED IN THE IOU-40

2G2	7426	2-Input NAND gate, open collector
2G10	74LSØØ	2-Input NAND gate
2G11	74LSØ2	2-Input NOR gate
4G5	74LS2Ø	Dual 4-Input NAND gate
4G6	74LS21	Dual 4-Input AND gate
COM3	74LS85	4-Bit Comparator
CTC	Z-8ØCTC	LSI Counter-Timer Circuit
CTR4	74LS161	4-Bit Synchronous Counter
FF2	74H74	Dual-D Flip-Flop
FF4	74LS74	Dual-D Flip-Flop
FF5	74LS273	Octal D-Type Flip-Flop
FF10	74LS373	Octal Latch with Tri-state Output
I2	7414	Inverter, Schmidt Trigger
I5	74LSØ4	Inverter
I6	74C9Ø1	CMOS Inverter/Driver
OD2	74LS138	Octal Decoder
OP6	34Ø3	Quad OP Amp
PD1	75451	Dual Power Driver
PGC2	74LS28Ø	9-Bit Parity Generator
RAM7	UPD416D	16K x 1 Bit Dynamic MOS RAM
RPROM2	27Ø8	1024 x 8 Bit Ultraviolet Eraseable ROM
SIO	Z-8ØSIO	LSI Serial Input/Output
TSB3	74LS24Ø	Octal Bus Buffer, Inverting, Tri-state
TSB4	74LS244	Octal Bus Buffer, Non-Inv., Tri-state

IOU-40 DOCUMENTS LISTING

A30719.......IOU-40 Design Specifications

A30840.......Asynchronous Front End for the IOU-40

A30841.......Bisynchronous Front End for the IOU-40

C30721.......D-Burn

C42085.......Fabrication

D30720.......IOU-40 Logic Drawings

F30719.......IOU-40 Hardware and Programming

L30719.......Scheduler Microcode

M42086.......Materials List

R42085.......Positive / Negative -- Artwork

IOU-40 OPERATIONAL NOTES

Performance of data exchange operations using the IOU-40 requires interaction between the on-board ROM (containing the Scheduler program), and the appropriate communications driver consisting of routines to allow interface to the user and facilitate the loading of the necessary object files into the IOU-40 Two-Port RAM to act as channel programs.

The Scheduler program acts as an arbitrator between channels in matters of channel activity, termination races, and interrupt handling. For data handling for each individual channel, the Scheduler accedes to the channel program in the Two-Port RAM, downloaded by the CPU following initialization. Control of the data exchange operation alternates between the Scheduler and the channel programs in the Two-Port RAM depending on the nature of the function involved. The CPU is made aware of changes in the data exchange process through the Status Ø register and the Interrupt line to the backplane. Both channels share the Interrupt line (the Scheduler providing coordination) and the IOU-40 is configured into the Qantel system as a Special Device.

Power-on or Reset Input/Output commands result in the IOU-40's Z-8Ø starting program execution at location $0000 in the ROM. The stack pointer is loaded, the Parity RAM is initialized, the Status Ø register is cleared, the channel activity and interrupt status bytes are reset to Ø, and the channel entry addresses are set to their initial value. The Z-8Ø, having completed these basic preparations, will periodically test the channel activity bytes to detect a change from $00 to $FF.

Meanwhile, the CPU must load the channel programs to be used into the Two-Port RAM and load the channel entry address with the starting location for each program. Once the channel

activity byte has been set by the CPU, the Scheduler will branch to the channel entry address and the data exchange takes place. In such case as both channels are active simultaneously, the Scheduler alternates between them to maintain an orderly data flow.

During the channel program execution, there are two ways in which control may be returned to the Scheduler: a task break call or an interrupt from the CTC. A task break call is initiated by the channel program executing an RST $30 instruction which acts as a call to location $0030. This gives the Scheduler the opportunity to check the status of the other channel.

An interrupt from the CTC occurs at 10 millisecond intervals. If the currently active channel has not responded within this time period, control is alternated to the other channel.

Control blocks stored in the Two-Port RAM can be altered by the main CPU at such times as the Control Block Present byte is set to $00. When the CPU enters new information into the Control Block area, it sets the Control Block Present byte to $FF to notify the channel program that updated information is ready for processing. As soon as the channel program enters these new variables into its activities, it sets the Control Block Present byte to $00 again.

Each time a channel wishes to signal termination, a set sequence of events takes place. All significant data involving the termination is stored in the appropriate Channel Status Block. The channel program then sets the Termination Request byte to the correct value: $FF to indicate a suspended termination or $0F to indicate a non-suspended termination. Control is then passed back to the Scheduler.

It is the Scheduler's duty, upon acknowledging the termination request, to check and ensure that a termination is not already pending. If not, it proceeds to raise the Interrupt in Status Ø and the flag for the channel signalling termination. If the ATI is set, the Interrupt line to the main CPU is pulled. If the channel is to be suspended, signified by the high bit in the Channel Termination byte, it will remain suspended until the main CPU issues a Read Status 2 command (resulting in the resetting of the Status Ø register).

In this manner, only one channel at a time may signal its termination to the main CPU, assuring that each Interrupt corresponds with one channel, and no termination attempts are lost.

DESCRIPTION OF THE TWO-PORT RAM VARIABLES

Allow Termination Interrupt Flag:

The main CPU sets and resets this flag with the following results to the IOU-40:

(1) If set to $FF, the Scheduler will notify the CPU of the termination of channel activity by pulling the Interrupt line to the backplane. At the same time, the Status Ø register is loaded with FLAG 1 high and the identification of the terminating channel.

(2) If set to $ØØ, the Interrupt line will not be pulled, but channel termination will be signified by FLAG 1 and the presence of the appropriate termination signal in Status Ø.

Scheduler Entry Point: (Ch A/ Ch B)

The Scheduler maintains this address, updating it at each task break or timer interrupt. During initialization it is set by the main CPU.

This location is loaded with the appropriate branch address for the given channel.

Activity Byte: (Ch A/ Ch B)

The main CPU modifies this byte.

$ØØ is an indication of an inactive channel. Any other value requires that the channel be serviced unless it is in a suspended status awaiting termination servicing.

Termination Status Byte: (Ch A/ Ch B)

The least significant bit in this byte is used to signal the CPU that the identified channel is requesting termination. The channel program sets the bit and the Scheduler responds by

16K RAM MEMORY MAP

$8000	Allow Termination Interrupt Flag
$8001 $8002	Ch A Scheduler Entry Point
$8003	Ch A Activity Byte
$8004	Ch A Termination Status Byte
$8005 $8006	Ch A Down Counter
$8007	Ch A Timer Running Byte
$8011 $8012	Ch B Scheduler Entry Point
$8013	Ch B Activity Byte
$8014	Ch B Termination Status Byte
$8015 $8016	Ch B Down Counter
$8017	Ch B Timer Running Byte
$801F	Transmit Clock Control Byte Copy
$8020 $80FF	Private Scratch Pad for Scheduler and Test Panel Code
$8100 $811E	Ch A Processor Control Block
$811F	Ch A Control Block Present Flag
$8120 $812F	Ch A Status Block
$8130 $81FF	Ch A Scratch Pad Area
$8200 $821E	Ch B Processor Control Block
$821F	Ch B Control Block Present Flag
$8220 $822F	Ch B Status Block
$8230 $82FF	Ch B Scratch Pad Area
$8300 $A0FF	Ch A Buffer & Programming Space
$A100 $BFFF	Ch B Buffer & Programming Space

Figure 6

loading Status Ø with FLAG 1, either FLAG 2 or 3 (to identify Channel A or B), and the Interrupt (if ATI is set, allowing it).

The most significant bit indicates the channel is suspended if the appropriate termination request bit is active. Resetting of Status Ø by the CPU will clear the Termination Status Byte and the channel will be scheduled.

Down Counter: (Ch A/ Ch B)

The program for the individual channel sets this counter value. The Scheduler decrements the count, as long as the Timer Running Byte is set, each 10 millisecond interval.

The value keeps track of the number of 10 millisecond intervals remaining before the Timer Running Byte will be reset to $ØØ.

Timer Running Byte: (Ch A/ Ch B)

This byte is set by the individual channel program and reset by the Scheduler.

$FF is the indication for the Down Counter to be decremented after each 10 millisecond interval.

Scheduler Private Scratch Pad:

This area of memory is dedicated to such uses as are necessary for the Scheduler program to perform specific functions and keep track of program activities. Also, particulars of test panel operation are stored here during test sequences.

Processor Control Block: (Ch A/ Ch B)

The CPU uses this area to relay to the given channel commands and various control information. The specifics and

definitions involved are a function of the individual channel program.

Control Block Present Flag: (Ch A/ Ch B)

$ØØ indicates that the control block has been processed. Any other value is a signal that new information is contained in the control block that needs to be incorporated into the channel program. The channel program will reset it to $ØØ following processing of the information.

Status Block: (Ch A/ Ch B)

Status of the individual channel is maintained in this area for scrutiny by the CPU at any time.

During routine operation, the status block is accessed at the time of channel termination. Specific definitions of addresses within the status block are determined by the individual channel program.

Scratch Pad Area: (Ch A/ Ch B)

This area of memory is left clear to be used in any manner required by the channel program.

Buffer and Programming Area: (Ch A/ Ch B)

This area defines the parameters within which the CPU can download the channel programs. The buffer zone provides an intermediary holding area for data being exchanged between the main CPU and other processors. It is important that channel programs and buffer space never exceed the expressed limitations of this area.

Transmit Clock Control Byte Copy

The last word written to perform the Transmit Clock Control operation is recorded at this location.

Z-8Ø INPUT/OUTPUT PORT DEFINITIONS

By issuing the specified IN and OUT instructions, the Z-8Ø activates the following control and data functions:

IN/OUT	$01-05........Test Panel	
IN/OUT	$40...........Channel A Data	
IN/OUT	$50...........Channel A Status and Control	
IN/OUT	$60...........Channel B Data	
IN/OUT	$70...........Channel B Status and Control	
IN/OUT	$80...........Channel A Speed Select	
IN/OUT	$81...........Channel B Speed Select	
IN/OUT	$82-83........Timer Interval Select	

Z-8Ø MEMORY-MAPPING DEFINITIONS

By performing Read or Write operations to the designated addresses, the Z-8Ø accesses portions of memory or status registers as listed:

READ	2K ROM..........................$0000-$07FF
WRITE	Status Ø Load..................$0800
WRITE	Transmit Clock Control..........$0C00
WRITE	Channel A Dialer Control........$1000
WRITE	Channel B Dialer Control........$1400
READ	Channel A/B Dialer Status.......$1800
READ	Status Ø Read..................$1C00
READ/ WRITE	16K Two-Port RAM................$8000-$BFFF

The following page defines individual bit designations that apply during memory-mapped operations.

REGISTER BIT SUMMARY

TRANSMIT CLOCK CONTROL (Z-80 Write to \$0C00)

Figure 7

2^0	Channel A Internal Transmit Clock Select
2^1	Channel B Internal Transmit Clock Select
2^2	undefined
2^3	undefined
2^4	undefined
2^5	undefined
2^6	undefined
2^7	undefined

(Note: In synchronous modes, selecting the internal clock consists of gating a CTC output to the channel transmit clock input and the connected modem.)

DIALER CONTROL (Channel A -- Write to \$1000)(Channel B -- Write to \$1400)

Figure 8

2^0	Number to be Dialed (1 Weight)
2^1	Number to be Dialed (2 Weight)
2^2	Number to be Dialed (4 Weight)
2^3	Number to be Dialed (8 Weight)
2^4	Digit Present
2^5	Set Call Request
2^6	Select Asynchronous Clock
2^7	Data Terminal Ready

CHANNEL A & B DIALER STATUS

Figure 9

2^0	Present Next Digit -- Channel A
2^1	Abandon Call & Retry -- Channel A
2^2	Data Line Occupied -- Channel A
2^3	Carrier Detected -- Channel A
2^4	Present Next Digit -- Channel B
2^5	Abandon Call & Retry -- Channel B
2^6	Data Line Occupied -- Channel B
2^7	Carrier Detected -- Channel B

STATUS Ø LOAD (Z-8Ø Write to $0800)

Figure 10

2^0	Set Loop Test Mode in IOU-40
2^1	Enable RAM Parity Circuits
2^2	Not Defined
2^3	Interrupt Line to Backplane (set if allowed)
2^4	FLAG 1 -- Termination Status
2^5	Channel A Termination Signal
2^6	Channel B Termination Signal
2^7	Inoperable (RAM Parity Error)

STATUS Ø READ (Z-8Ø Read of $1C00)

Figure 11

2^0	undefined
2^1	undefined
2^2	undefined
2^3	undefined
2^4	FLAG 1
2^5	Channel A Termination Signal
2^6	Channel B Termination Signal
2^7	RAM Parity Error (set by hardware)

STATUS 0 REGISTER

(AS SEEN BY THE MAIN CPU)

Figure 12

2^0	READ BUSY
2^1	WRITE BUSY
2^2	END
2^3	SERVICE REQUEST
2^4	FLAG 1 TERMINATION STATUS / INTERRUPT
2^5	CHANNEL A TERMINATION SIGNAL
2^6	CHANNEL B TERMINATION SIGNAL
2^7	INOPERABLE / RAM PARITY ERROR

MESSAGE FORMATS

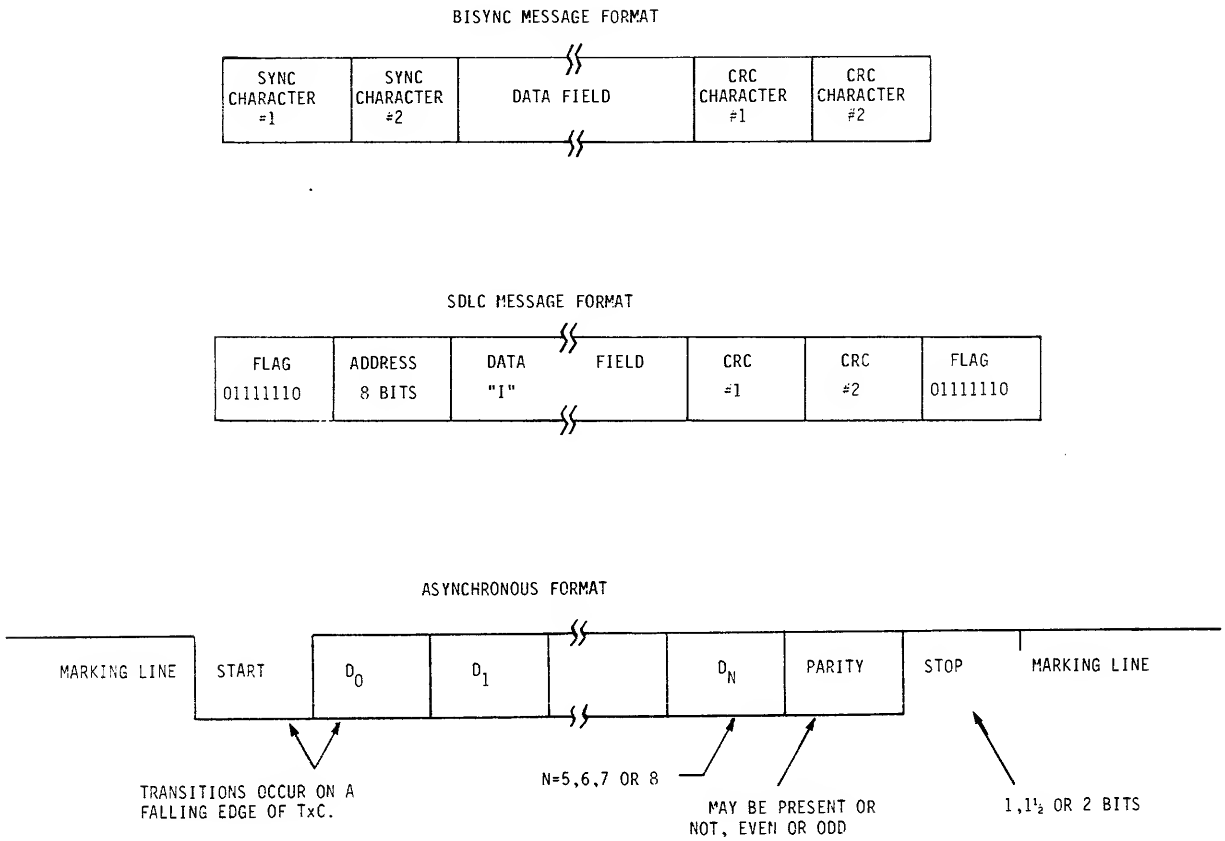
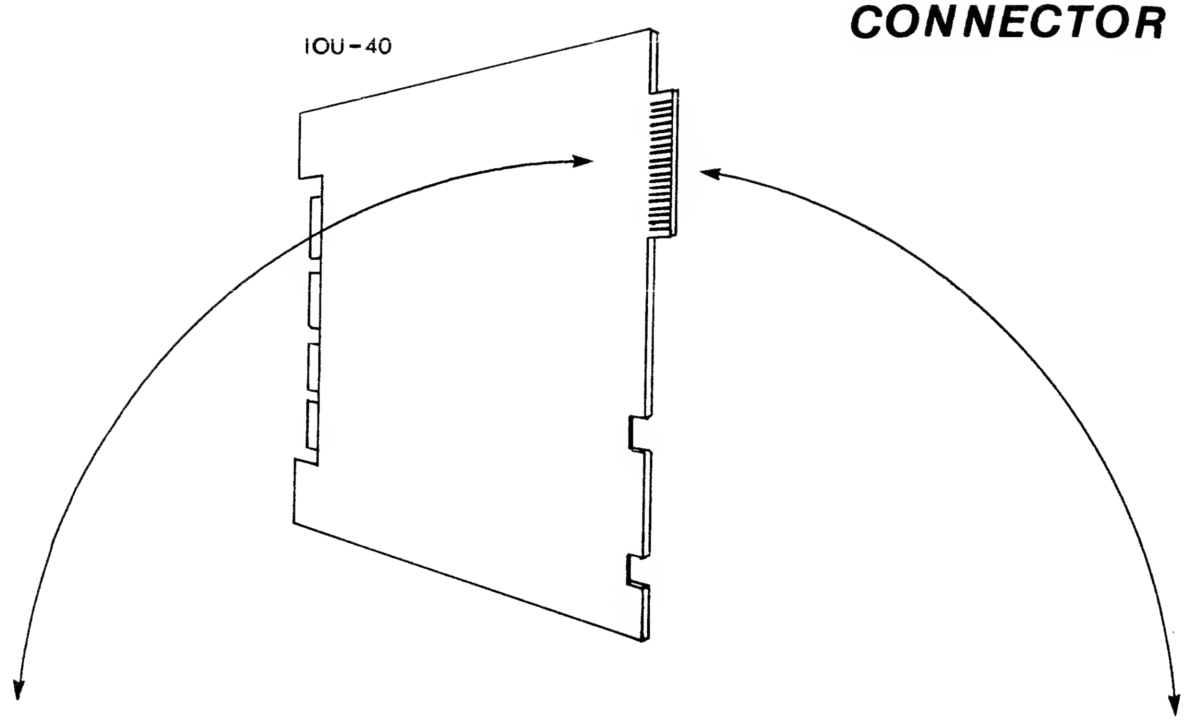


Figure 13

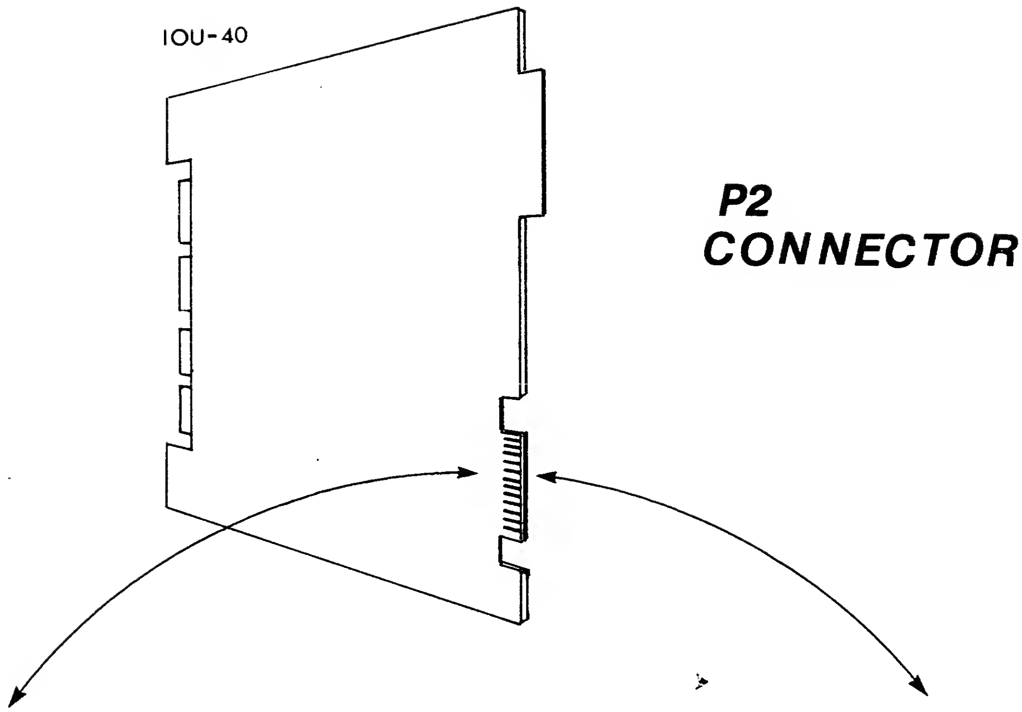
The three basic message formats handled by the IOU-40 communications controller are illustrated here. Control signals sent to the Z-8Ø SIO by the Z-8Ø microprocessor based on information the Z-8Ø obtains from the Two-Port RAM (loaded by the main CPU) condition the SIO to handle the intricacies of the data transfer whatever message format is being used. Although it is beyond the scope of this manual to discuss the specific details of each format, references listed in the bibliography provide more information about these matters.

P1 CONNECTOR



PIN #1	+5V	+5V	PIN #2
3	STROBE-N	GND (OV)	4
5	+12V	IOE0-N	6
7	IOE1-N	IOE2-N	8
9	IOE3-N	GND (OV)	10
11	INT-N	GND (OV)	12
13	IOB00-P	IOB01-P	14
15	IOB02-P	IOB03-P	16
17	IOB10-P	IOB11-P	18
19	IOB12-P	IOB13-P	20
21	GND (OV)	GND (OV)	22
23	GND (OV)	GND (OV)	24
25	PFL-N	GND (OV)	26
27	-12V	SRES-N	28
29	+26V	+26V	30

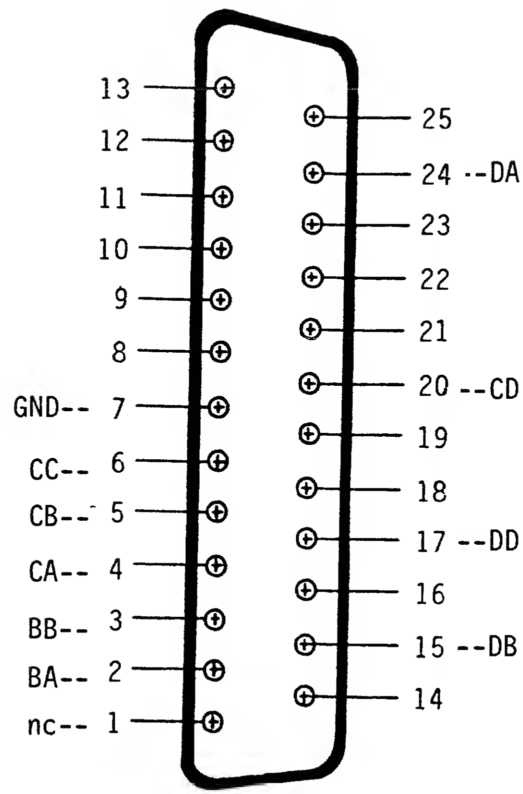
Figure 14



PIN #1	GND (OV)	GND (OV)	PIN #2
3	+5V	+5V	4
5	IORQ-N	BUSAK-N	6
7		RD-N	8
9	AD06-P	RES-N	10
11	AD01-P	AD07-P	12
13	AD03-P	AD00-P	14
15	IORD-P	AD05-P	16
17	MREQ-N	WR-N	18
19	MONE-N	AD04-P	20
21	RFSH-N	AD02-P	22
23	IOWR-P	NMI-N	24
25	DA6-P	AD12-P	26
27	DA1-P	AD14-P	28
29	DA0-P	AD08-P	30
31	DA4-P	AD15-P	32
33	DA5-P	AD09-P	34
35	DA3-P	AD10-P	36
37	DA2-P	AD11-P	38
39	DA7-P	AD13-P	40
41	BUSRQ-N	ZINT-N	42
43	HALT-N	WAIT-N	44
45	CLK-P	FASTCLK-P	46
47	+5V	+5V	48
49	GND (OV)	GND (OV)	50

Figure 15

P3 (Channel A) & P4 (Channel B)

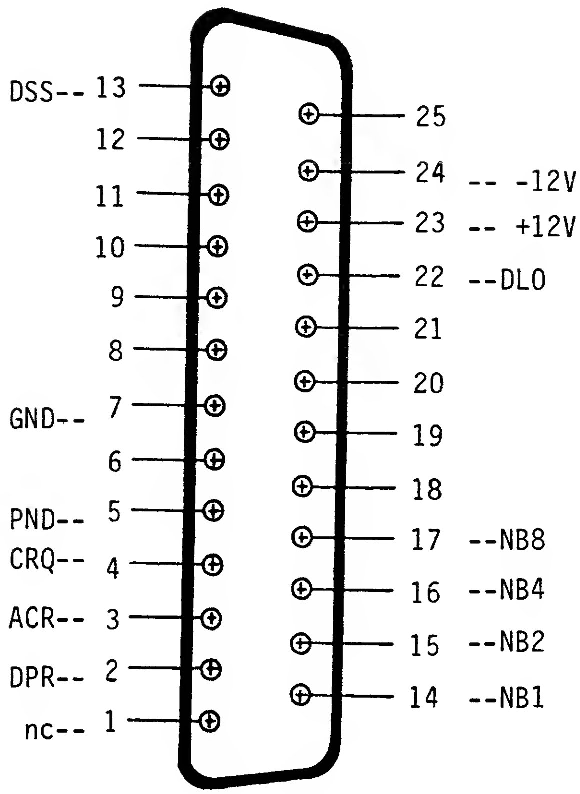


KEY TO SIGNALS

Pin #	Signal	Meaning
1	nc	Chassis Strap (not connected to ground)
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
7	GND	Øv
15	DB	Transmitter Signal Element Timing to DTE
17	DD	Receiver Signal Element Timing
20	CD	Data Terminal Ready
24	DA	Transmitter Signal Element Timing to DCE

Figure 16

P5 (Channel A) & P6 (Channel B)



KEY TO SIGNALS

Pin #	Signal	Meaning
1	nc	Chassis Strap (not connected to ground)
2	DPR	Data Present Strobe
3	ACR	Abandon Call and Retry
4	CRQ	Call Request
5	PND	Present Next Digit
7	GND	Øv
13	DSS	Data Set Status

Pin #	Signal	Meaning
14	NB1	Weighted Binary Value (1)
15	NB2	Weighted Binary Value (2)
16	NB4	Weighted Binary Value (4)
17	NB8	Weighted Binary Value (8)
22	DLO	Data Line Occupied
23	+12V	Supply Voltage
24	-12V	Supply Voltage

Figure 17

TEST PROGRAMS FOR THE IOU-40

This section contains descriptions of several test programs designed for use in conjunction with the IOU-40. The first two programs will be present on the release tape prepared for the IOU-40 (COM40.X). The second set of programs will be released as ATP's.

*LOOP40 -- IOU-40 Loopback Test Program

Purpose: To allow automatic testing of the major hardware components of the IOU-40 and system interfaces (including modems and other RS-232 devices and related cabling). This is accomplished by downloading a test program into the Two-Port RAM (which is read back by the CPU to check for any errors in the data transfer). The CPU then issues a series of commands and monitors the response of the IOU-40. Channel A or Channel B (as selected by the operator) inputs and outputs are looped together at one of the following stages --

> At the board, using a single channel loopback test fixture (Part #A42406-1).
>
> At the end of a connected RS-232/V24 cable (utilizing the same loopback test fixture connected to the male end of the cable).
>
> At the modem (with analog loopback test function operating).
>
> At a remote modem (separated by a telephone line and related modem) using the digital loopback test function.

These options allow the troubleshooter to isolate improperly functioning communication links, as well as establishing the operability of the IOU-40.

*LOOP40 CONTINUED

Operator Input: With the IOU-40 configured under BEST as a special device, the following sequence of operator steps should be followed --

TERMINAL DISPLAY	OPERATOR RESPONSE
READY	RUN *LOOP40
Month-Day-Year IOU-40 LOOPBACK TEST PROGRAM - DEVICE NAME:	Enter the 3-character designation for the IOU-40 (as configured)
CONTINUOUS TEST? (Y/N)	A Yes (Y) response will cause automatic repetition of the testing until terminated by the operator (Flag 3/Transmit)
CHANNEL TO BE TESTED? (A/B)	Enter the choice for the channel to be tested -- A or B

At this point, the operator needs merely to observe the displayed results. Tests performed and possible indications are:

TEST	POSITIVE RESULT	ERROR INDICATION
DOWNLOAD	SUCCESSFUL	ERROR ON LOADING MICRO-CODE or ERROR ON READING IOU-40 BACK
STATUS Ø TEST	SUCCESSFUL	FAILED
TIMER INTERRUPT TEST	SUCCESSFUL	FAILED

*LOOP40 CONTINUED

TEST	POSITIVE RESULT	ERROR INDICATION
SET DTR/DSR	SUCCESSFUL	FAILED
RESET DTR/DSR	SUCCESSFUL	FAILED
SET RTS/CTS	SUCCESSFUL	FAILED
RESET RTS/CTS	SUCCESSFUL	FAILED
INT TRANSMIT CLOCK	SUCCESSFUL	FAILED; CAN'T SHIFT OUT CHARACTER
EXT TRANSMIT CLOCK	SUCCESSFUL	FAILED; CAN'T SHIFT OUT CHARACTER
SYNC DATA LOOPBACK	SUCCESSFUL	FAILED; NO SYNC CHARACTER DETECTED or
		FAILED; DATA ERROR or
		FAILED; NO DATA TIME OUT
ASYNC DATA LOOPBACK	SUCCESSFUL	FAILED: DATA ERROR or
		FAILED; NO DATA TIME OUT

If continuous testing was not specified, test concludes at this point with the display: LOOPBACK TEST COMPLETE.

*ETP40 -- TWO CHANNEL LOOPBACK TEST FOR THE IOU-40

Purpose: To perform basic functional testing of the IOU-40 hardware and interface to the CPU. Data is exchanged between Channel A and Channel B through two BEST partitions maintaining IBM bi-sync protocol requirements. Channel A will display its received data on the terminal; Channel B, on an attached printer.

Prerequisites for test operation: Successful operation of this test procedure requires the following --

A Qantel system providing a minimum of two 8K partitions under BEST with a terminal and a line printer.

IOU-40 controller configured into the system as a Special Device (without Interrupt or DMA capabilities). Channels should be identified as A40 and B40.

Bi-sync microcode for the two channels as contained within two standalone object files -- !BSC40A and !BSC40B.

Emulator programs for 2780 activity as contained within BEST object files (foreground and background -- *ETP40 and *ETP40B).

Test fixture A42406-2, the two channel loopback device, used for interchannel data and modem signal exchange.

Operator input: With the terminal READY indication, the operator should enter: RUN *ETP40. At this point, the program will attempt to activate the foreground and background partitions with the appropriate object files for test operation, pausing to request the operator press the TRANSMIT key after each loading.

Following completion of this step, a pattern will be alternately displayed on the terminal (Channel A's data) and the printer (Channel B's data). Errors in accomplishing any of the necessary steps for execution will result in the display of an error indication, and, in some cases, an error code which will specify details of the failure. The error codes are described in the following table.

*ETP40 CONTINUED

ERROR CODES FOR *ETP40

01.......Unable to open transmit. Line bid unsuccessful due to no response or incorrect response following several retries.

02.......Incorrect response.

03.......Repeated data errors resulting in excess NAK's.

04.......No response.

06.......EOT received following receive error.

90.......Open exception at startup. IPL system to disable microcode currently running in the IOU-40.

99.......Fatal hardware error. At startup: failure to signal termination within 1 second of CPU's initialization command. After initialization: Clear to Send was not active within 300 milliseconds of the time Request to Send was set by the channel program.

DESCRIPTION OF ATP'S FOR THE IOU-40

The ATP's described in this section perform individualized testing of specific aspects of the IOU-40. They operate in a standalone capacity and are loaded using the standard ATP loading procedure.

CTC40 -- Test for the Counter-Timer Circuit in the IOU-40

Purpose: To test the operability of the Z-8Ø CTC chip and exercise all associated control and data lines involved with it.

Program Sequence

Checks IOU-40 identity by issuing a Read Status 2 command.

CTC40 CONTINUED

Program Sequence

Downloads Z-8Ø microcode into the Two-Port RAM and then reads back the code to check accuracy.

IOU-40 begins executing Z-8Ø microcode.

CTC is initialized.

Interrupt Mode 2 is set.

Prescalars and counts are generated to produce predetermined timing intervals. Intervals are measured against known periods for accuracy.

Testing is structured to exercise all four ports -- $80, $81, $82, and $83.

Testing continues until halted by the operator pressing Flag 3.

SPECIAL NOTE: Due to the format of the microprogram for this test procedure, no device within the system is allowed to interrupt the CPU while the program is being executed.

CPU40 -- Test for Z-8Ø Microinstruction Functioning

Purpose: To test all Z-8Ø microinstructions that can be run on the IOU-40 excluding I/O instructions. This test program is designed to be run with Q7.5 processors and requires 32K of CPU memory.

Program Sequence

Checks IOU-40 identity by issuing a Read Status 2 command.

Requests that the operator input a value for the number of test repetitions: ITERATION COUNT (HHHH): *Operator should respond with a 4-digit hex number. Default value if the operator fails to specify and simply hits carriage return is $100.*

CPU40 CONTINUED

Program Sequence

Program asks: HALT AFTER ERROR? *The operator may respond with Flag 2 for yes or Flag 3 for no.*

Program asks: REPEAT TEST? *Operator should press Flag 2 if desiring continuous testing.*

Downloads Z-8Ø microcode into the Two-Port RAM. Test execution normally begins at this point. If the IOU-40, however, does not respond, the HALT light will be activated and the message displayed: NO RESPONSE FROM IOU-40, HIT ST/SP TO RETRY. *Pressing the Start/Stop button reloads the microprogram.*

Testing is performed and instructions being executed are displayed on the terminal accompanied with the appropriate object code. The detection of an error results in the display of contents of all the Z-8Ø registers.

While testing is underway, the operator may obtain the current iteration value by pressing Flag 2. Flag 3 will terminate execution at the conclusion of the current test.

The detection of an error will halt the CPU. The current test may be continued by pressing the Start/Stop button. A combination of Flag 3 and Start/Stop being activated results in the current test being skipped and the program proceding with the next instruction test.

SIO -- Test for Z-8Ø SIO Functioning

Purpose: To test the functioning of the Z-8Ø SIO within the normal operating parameters of the IOU-40 by exchanging data between Channel A and Channel B in a variety of communication modes. This test program is designed to be run with a Q7.5 processor and requires 16K of CPU memory. The connectors P3 and P4 are looped together with the test fixture A42406-2.

Program Sequence

Checks IOU-40 identity by issuing a Read Status 2 command.

Program asks: HALT AFTER ERROR? *The operator may respond with Flag 2 for yes or Flag 3 for no.*

Program asks: REPEAT TEST? *For continuous testing, the operator should answer with Flag 2 for yes.*

Downloads Z-8Ø microcode into the Two-Port RAM. Microcode is read back by the CPU to check for accuracy. The IOU-40 can begin executing the microcode as soon as the CPU writes an $FF to the Channel A Activity Byte (location $8003).

Testing proceeds with the following individual checks:

Set Data Terminal Ready / Data Set Ready for Channels A and B.

Reset Data Terminal Ready / Data Set Ready for Channels A and B.

Set Ready to Send / Clear to Send for Channels A and B.

Reset Ready to Send / Clear to Send for Channels A and B.

Internal Transmit Clock tested at 19,200 bits per second for Channel A and B.

External Transmit Clock tested as above. Since no connection is made at pin 15 of the RS-232 interface, this test will indicate a failure.

Internal Receive Clock tested at 19,200 bits per second for Channels A and B.

External Receive Clock tested for Channels A and B.

The program continues by conditioning the SIO for the synchronous mode of data transmission at 19,200 bits per second. Data is sent from Channel A to Channel B, excluding sync bits, and monitored for correct transmission. Channel B then transfers data to Channel A. Errors are reported as they occur.

The program then conditions the SIO for asynchronous mode of transmission at 19,200 bits per second. Data is shifted from Channel A to Channel B while the status is constantly monitored. Channel B then transfers data to Channel A.

Errors are reported in any particular test sequence as they occur. *The operator may restart a halted system following an error by pressing Start/Stop. This causes the program to attempt to repeat the current test block. Activating Flag 3 and pressing Start/Stop causes the test under execution to be skipped and the program to continue with the next test in the sequence. Activating Flag 2 and pressing Start/Stop will repeat a test under execution without reporting errors that were detected initially during the testing process.*

BIBLIOGRAPHY

Eason, Tom S., et al. Fundamentals of Data Communications. New York: John Wiley and Sons, 1978.

McNamara, John E. Technical Aspects of Data Communications. Bedford, Mass.: Digital Press, 1978.

IBM Systems Reference Library -- Binary Synchronous Communications -- TP-09 A27-3004-0.

The following manuals are available from Zilog, 10340 Bubb Road, Cupertino, California 95014.

Z-8Ø Data Book *containing product specifications of Z-8Ø family of MOS LSI microcomputer components.*

Z-8Ø SIO Product Specification

Z-8Ø CTC Technical Manual

Z-8Ø CPU Technical Manual

Z-8Ø Assembly Language Programming Manual

INDEX TO THE LOGIC DRAWINGS

IOU-40 ACRONYMS

A............A-bus -- Multiplexed 7-bit address bus to the Two-Port RAM.

ACUA/
ACUB.........Automatic Call-Up A & B -- Memory-mapped signals for latching data into the Channel A or B Auto-Call flip-flops.

AD...........AD-bus -- Address bus of the Z-8Ø.

AD15.........The highest order address line used as a memory-map cue to enter the Two-Port RAM.

BUSAK........Bus Acknowledge -- Issued by the Z-8Ø upon receipt of request to clear all bus lines for outside access.

BUSRQ........Bus Request -- Signal derived from CPU issued SRD or SWR to initiate a READ or WRITE operation by requesting bus access from the Z-8Ø.

CAD-ØP/
CAD-1P.......Column Address Enable -- Timing signals used to periodically direct the high or low order portions of the Address Counter or the Z-8Ø Address bus to the A-bus.

CAS-ØP/
CAS-1P.......Column Address Strobe -- Timing signal for latching the higher order bits from the Address Counter or the Z-8Ø Address bus to the RAM memory chips.

CLK..........Clock -- Derived from on-board crystal oscillator, a 2.4576 MHz square wave used for system synchronization.

COUNT........Signal used to increment the Address Counter.

DA...........8-bit unidirectional data bus.

DB...........Buffered 8-bit unidirectional data bus.

FASTCLK......High speed clock running at twice the Z-8Ø cycle time.

IOB..........8-bit bidirectional data bus with the CPU via backplane.

IOE..........4-bit control signal bus from CPU via backplane.

IORQ.........Signal to indicate that lower half of the address bus holds a valid Input/Output address.

LOOP.........Signal enabling a buffer to create a Channel A feedback loop for test purposes.

MREQ.........Memory Request -- Z-8Ø issued control signal involved with the access of memory.

MOSCLK.......2.4576 MHz clock signal to the SIO chip for synchronization of data flow.

PEN..........Parity Enable -- Memory-mapped signal to prepare parity checking circuit for operation.

PER..........Parity Error -- Output of parity checking circuit indicating an error.

RAS..........Row Address Strobe -- Timing signal for latching the lower order bits from the Address Counter or the Z-8Ø Address bus to the RAM memory chips.

IOU-40 ACRONYMS

RD...........Read -- Z-8Ø signal requesting data.

RDD.........READ DATA -- A control signal used by the CPU to extract a byte of data from the Read register.

REF..........D.C. reference voltage for all comparators.

RES..........RESET -- Hardware reset from the backplane.

RFSH.........Refresh -- A Z-8Ø signal used in refresh operations of dynamic RAM.

RIO..........RESET I/O issued by CPU on IOE bus.

ROMØ/
ROM1.........Memory-mapped signals to select one of the two ROM chips.

RSØ..........READ STATUS Ø issued by CPU on IOE bus.

RS2..........READ STATUS 2 issued by CPU on IOE bus.

RS2-NS.......A derivative of READ STATUS 2 used to clear Status Ø register.

RUN..........Extended reset pulse routed to Z-8Ø chips and transmit clock circuits.

SØH..........Status Ø High -- A Z-8Ø write operation to location $0800 produces SØH, the clock signal for loading the Status Ø register.

SØI..........Status Ø Input -- Memory-mapped signal to allow the Z-8Ø to read the high Status Ø register.

SCLK.........Select Clock -- Memory-mapped signal to clock flip-flops for selecting internal or external transmit clocks.

SRD..........SET READ issued by CPU on IOE bus to initiate data transfer.

STROBE.......Timing signal issued by CPU to validate control signals and data transfers.

SWR..........SET WRITE issued by CPU on IOE bus to initiate data transfer.

TACU.........Memory-mapped enable signal for routing incoming Auto-Call status information to the Z-8Ø.

TER..........TERMINATE issued by CPU on IOE bus.

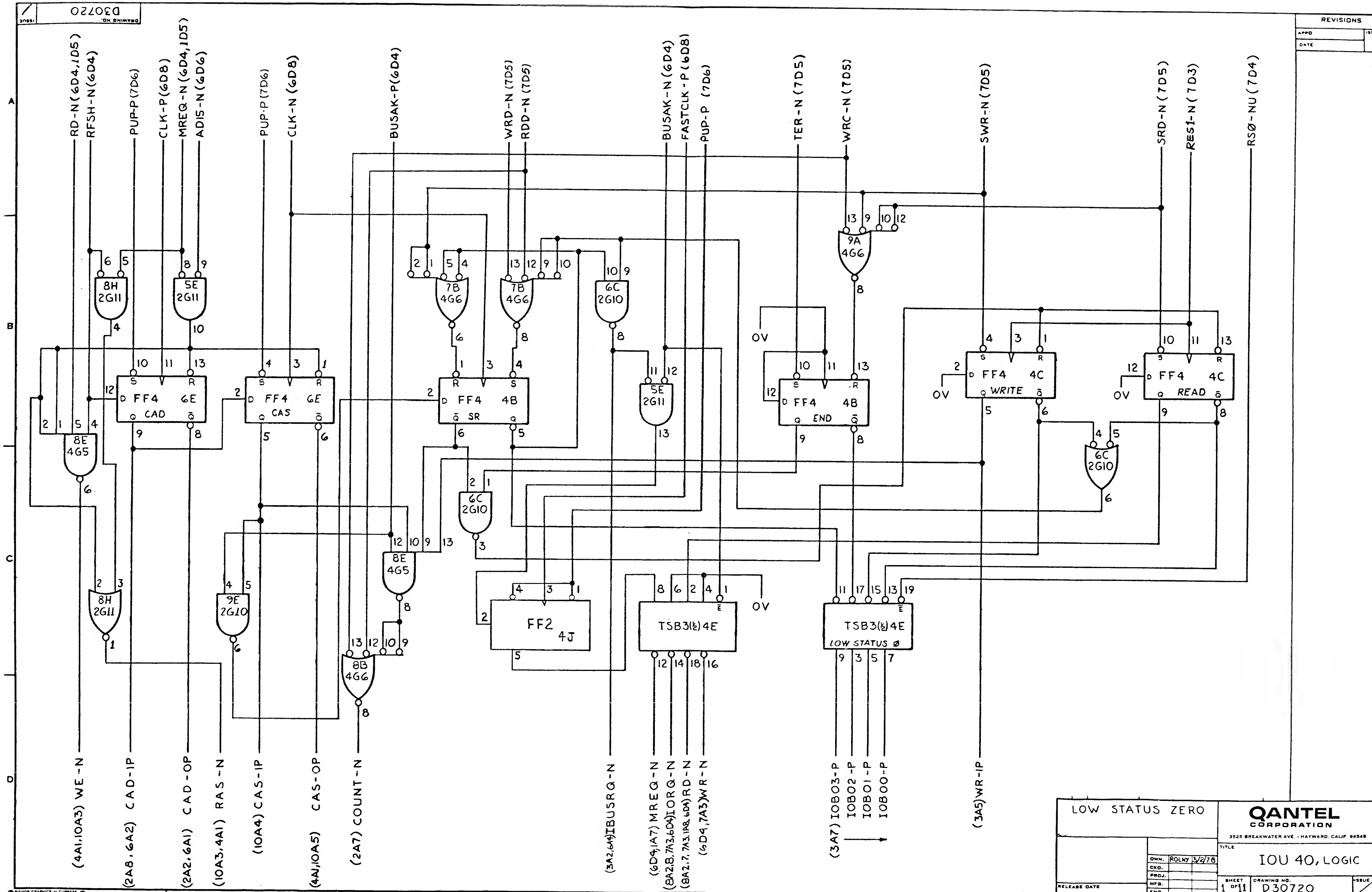
TxCA/
TxCB.........Transmit Clock A & B -- Timing signal to the transmit register of the SIO.

WR-1P........Write -- A control signal generated to enter data into the Write register. The 'Q' output of WR BUSY in Status Ø.

WRC..........WRITE CONTROL issued by CPU on IOE bus to load values into the Address Counters.

WRD..........Write Data -- A control signal used by the CPU for loading the Write register with a byte of data.

ZINT.........Z-8Ø Interrupt -- CTC generated signal to interrupt the Z-8Ø at timeout.



REVISIONS

LOW STATUS ZERO

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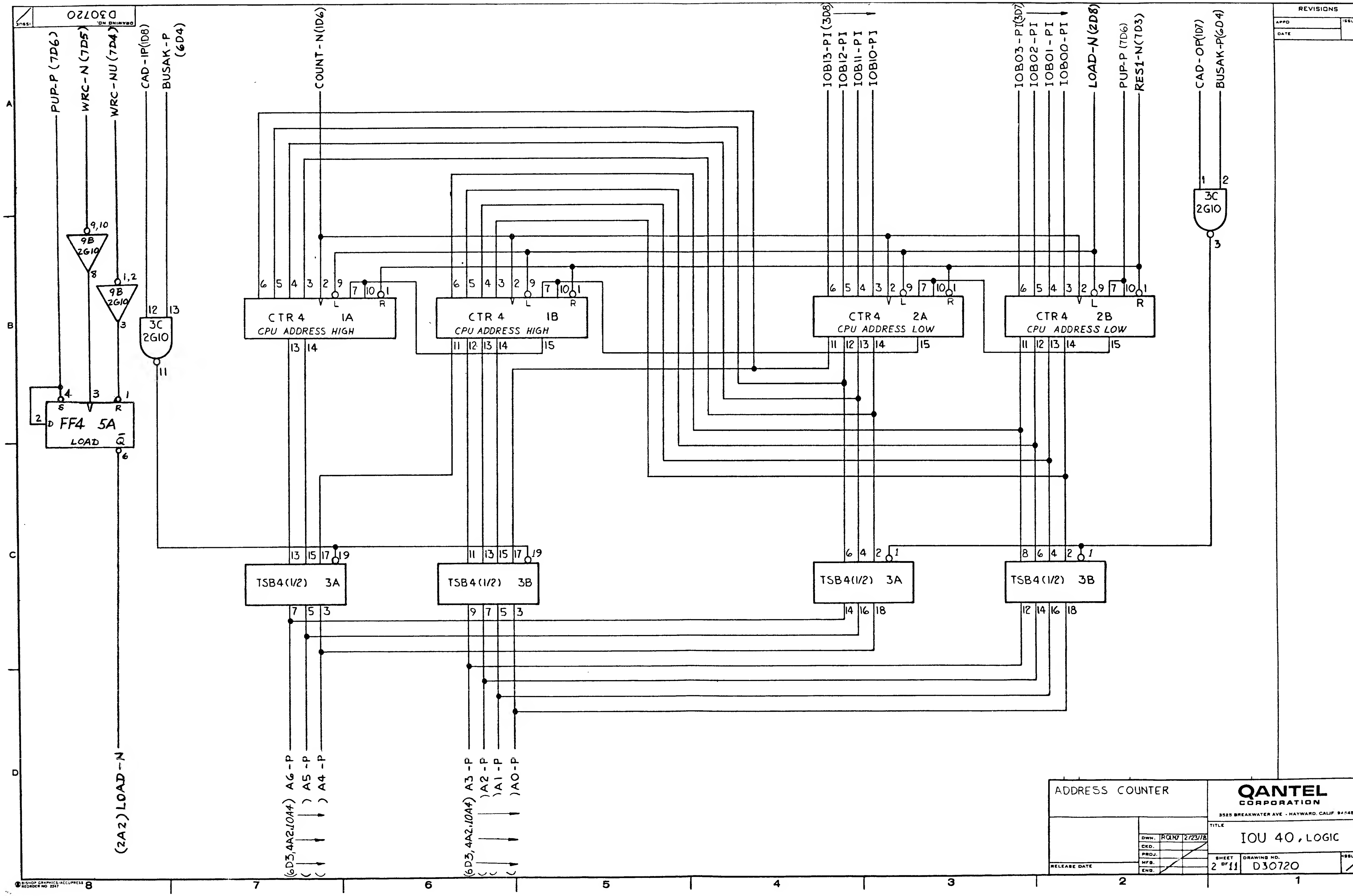
TITLE: IOU 40, LOGIC

DWN. ROLNY 3/2/78

SHEET 1 OF 11 — DRAWING NO. D30720

RELEASE DATE


D30720
PUP-P (7D6)
WRC-N (7D5)
WRC-NU (7D4)
CAD-IP(1D8)
BUSAK-P (6D4)
COUNT-N(1D6)
IOB13-PI(3D8)
IOB12-PI
IOB11-PI
IOB10-PI
IOBO3-PI(3D7)
IOBO2-PI
IOBO1-PI
IOBOO-PI
LOAD-N(2D8)
PUP-P (7D6)
RES1-N(7D3)
CAD-OP(1D7)
BUSAK-P(6D4)
9B 2G10
3C 2G10
FF4 5A
LOAD
CTR4 1A
CPU ADDRESS HIGH
CTR4 1B
CPU ADDRESS HIGH
CTR4 2A
CPU ADDRESS LOW
CTR4 2B
CPU ADDRESS LOW
TSB4(1/2) 3A
TSB4(1/2) 3B
(2A2) LOAD-N
(6D3,4A2,10A4) A6-P
A5-P
A4-P
(6D3,4A2,10A4) A3-P
A2-P
A1-P
A0-P
REVISIONS
ADDRESS COUNTER
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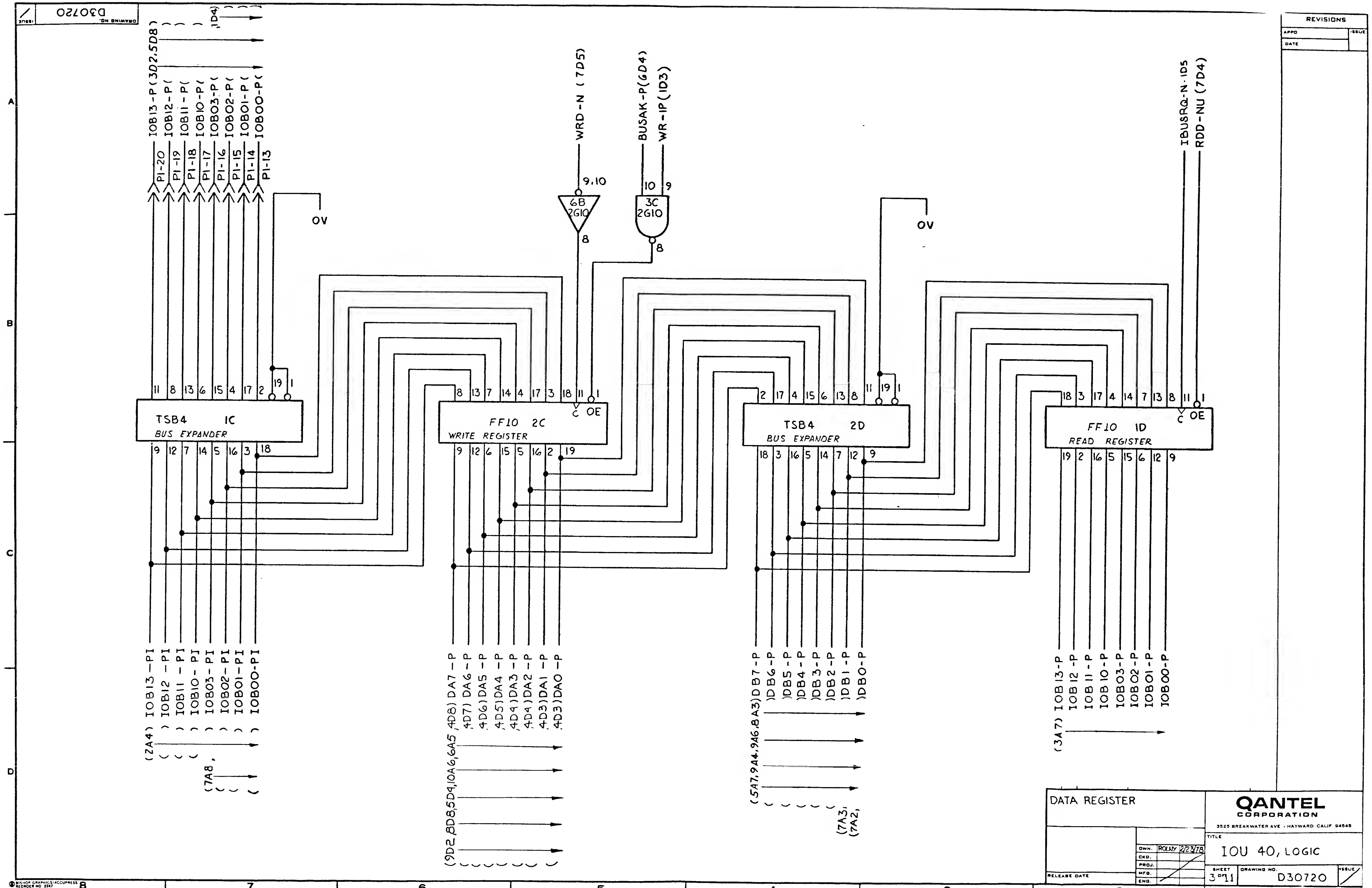
DWN. RQN 2/23/78
SHEET 2 OF 11
DRAWING NO. D30720


IOB13-P(3D2,5D8)
IOB12-P(
IOB11-P(
IOB10-P(
IOB03-P(
IOB02-P(
IOB01-P(
IOB00-P(
P1-20
P1-19
P1-18
P1-17
P1-16
P1-15
P1-14
P1-13
0V
WRD-N (7D5)
BUSAK-P(6D4)
WR-IP(1D3)
6B 2G10
3C 2G10
IBUSRQ-N·1D5
RDD-NU (7D4)
TSB4 1C
BUS EXPANDER
FF10 2C
WRITE REGISTER
TSB4 2D
BUS EXPANDER
FF10 1D
READ REGISTER
C
OE
(2A4) IOB13-P1
IOB12-P1
IOB11-P1
IOB10-P1
IOB03-P1
IOB02-P1
IOB01-P1
IOB00-P1
(7A8,
(9D2,8D8,5D4,10A6,6A5,4D8) DA7-P
4D7) DA6-P
4D6) DA5-P
4D5) DA4-P
4D4) DA3-P
4D4) DA2-P
4D3) DA1-P
4D3) DA0-P
(5A7,9A4,9A6,8A3) DB7-P
DB6-P
DB5-P
DB4-P
DB3-P
DB2-P
DB1-P
DB0-P
(7A3,
(7A2,
(3A7) IOB13-P
IOB12-P
IOB11-P
IOB10-P
IOB03-P
IOB02-P
IOB01-P
IOB00-P
REVISIONS
DATA REGISTER
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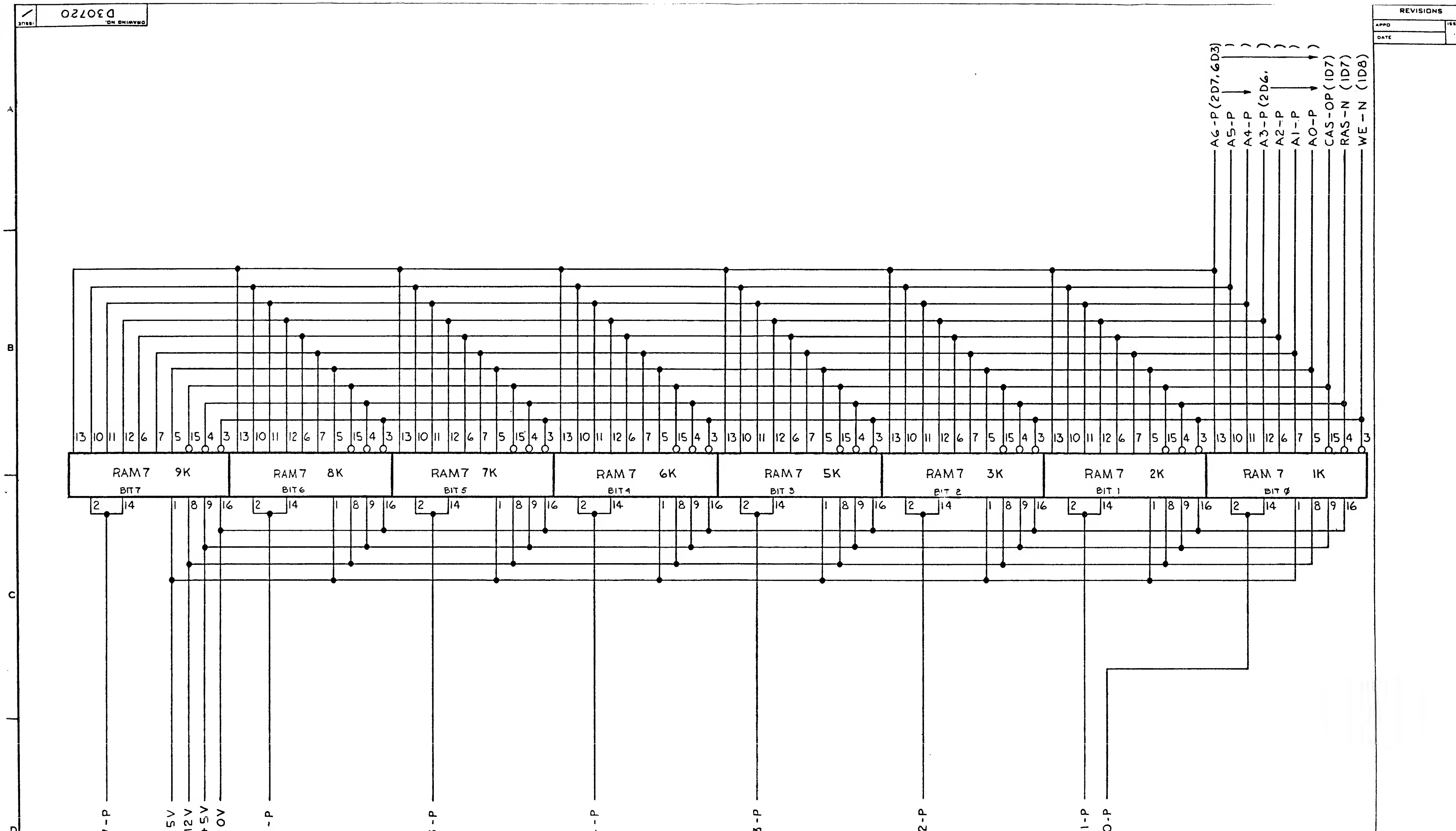
DRAWING NO. D30720



16K BYTE DYNAMIC RAM

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CKD.

PROJ.

MFG.

ENG.

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SHEET 4 OF 11

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ISSUE

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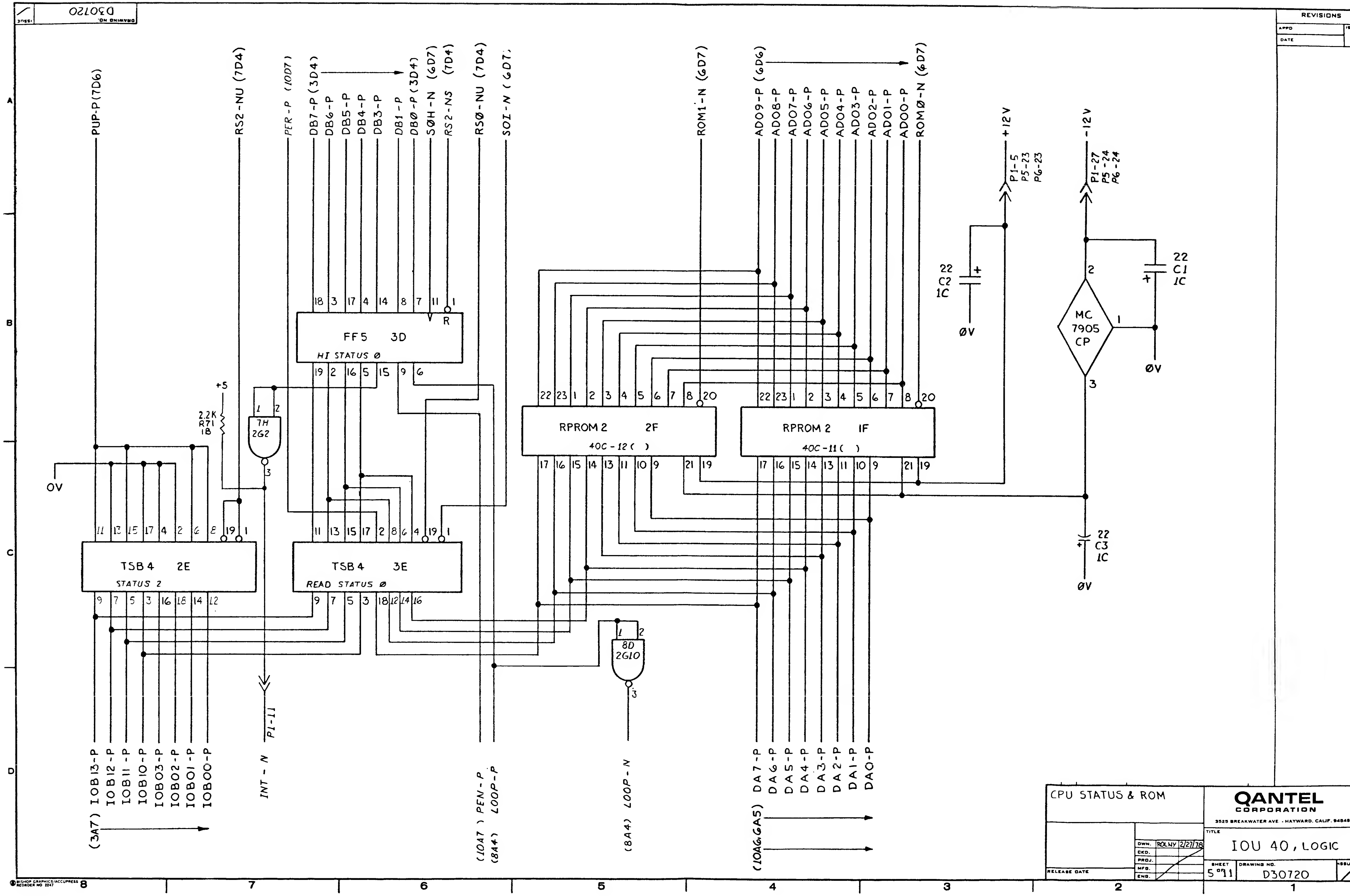

CPU STATUS & ROM

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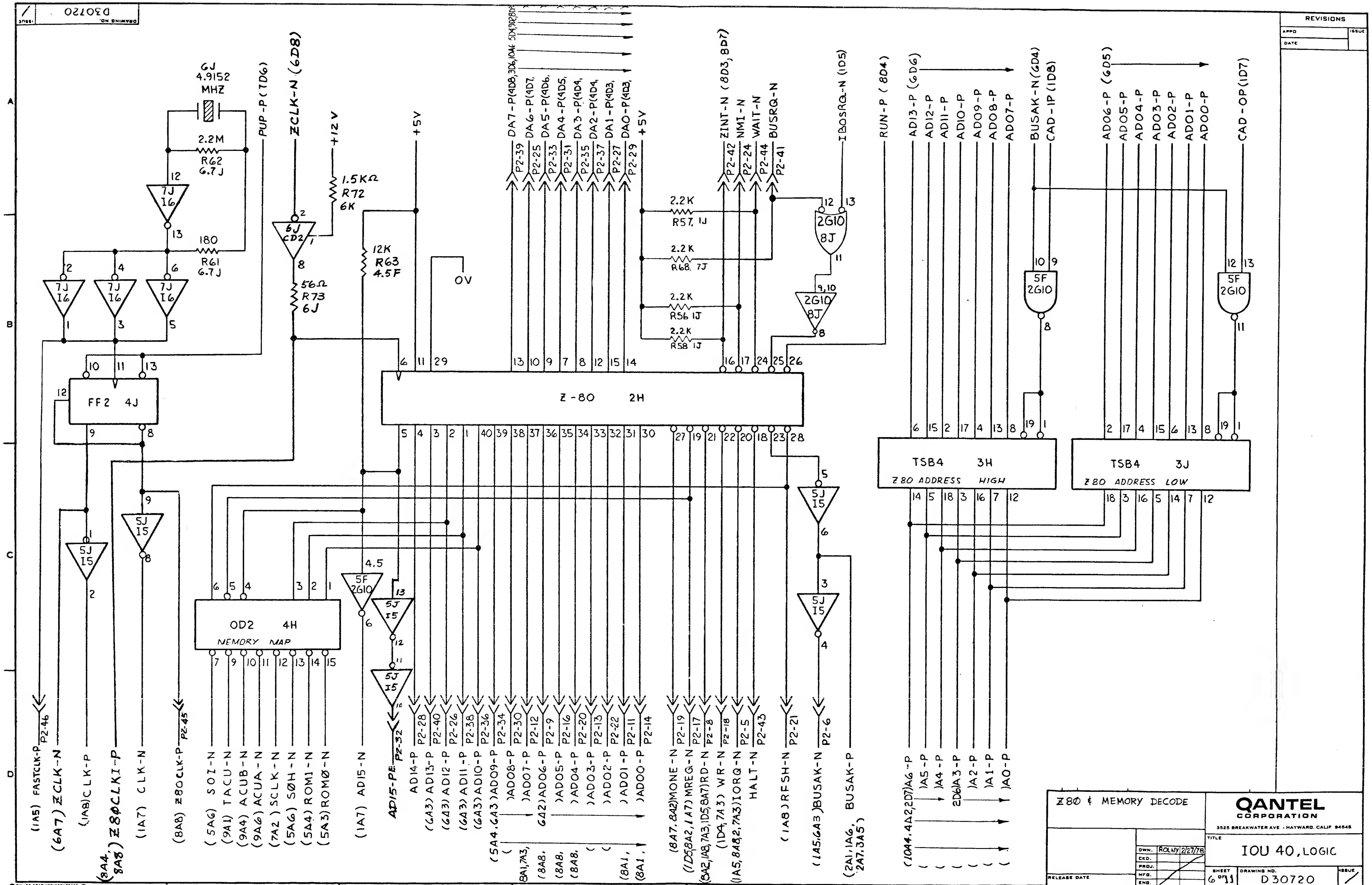

Z80 & MEMORY DECODE
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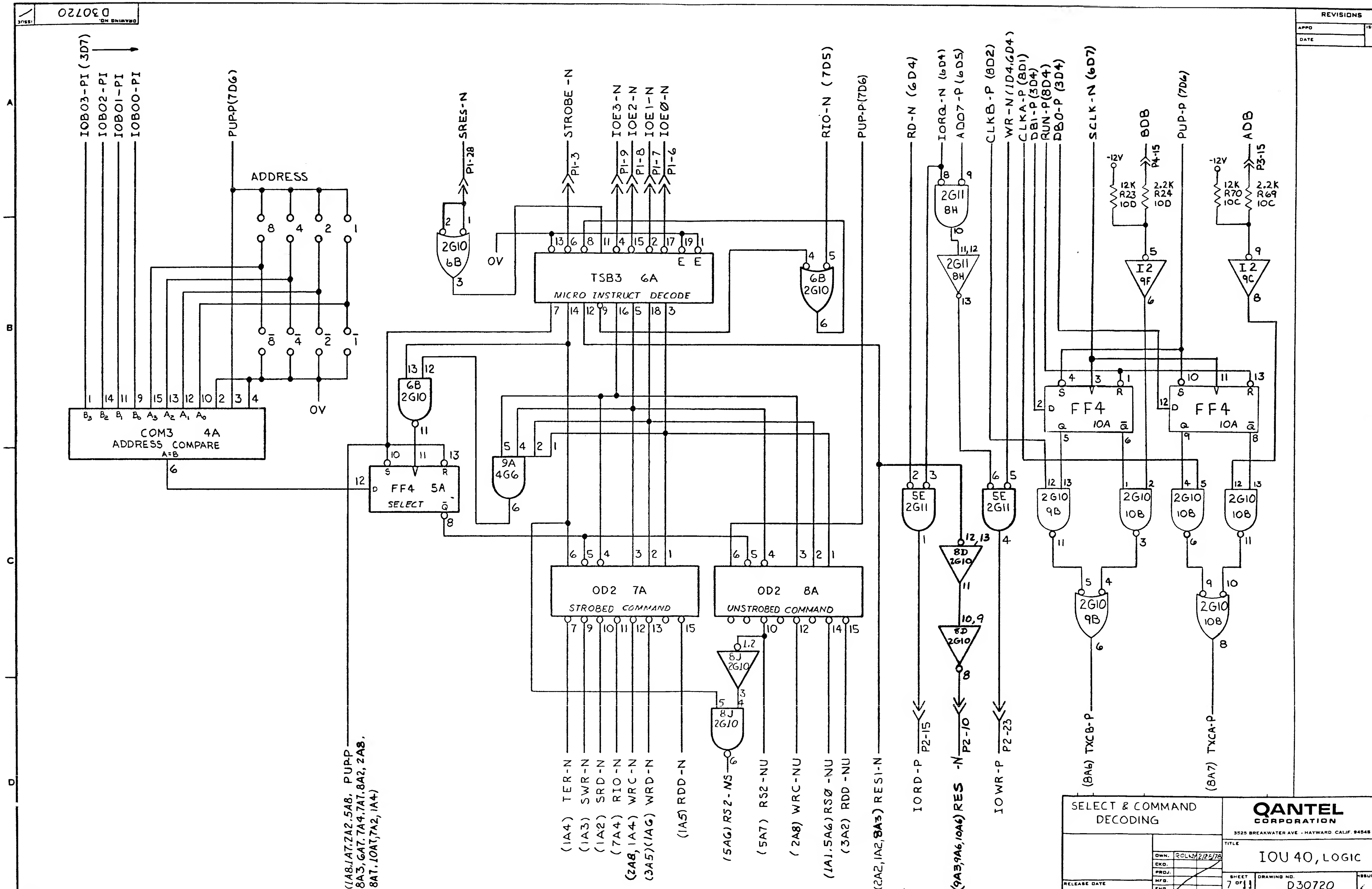
IOU 40, LOGIC
D30720
Z-80 2H
TSB4 3H Z80 ADDRESS HIGH
TSB4 3J Z80 ADDRESS LOW
OD2 4H MEMORY MAP
FF2 4J
6J 4.9152 MHZ
REVISIONS



SELECT & COMMAND DECODING

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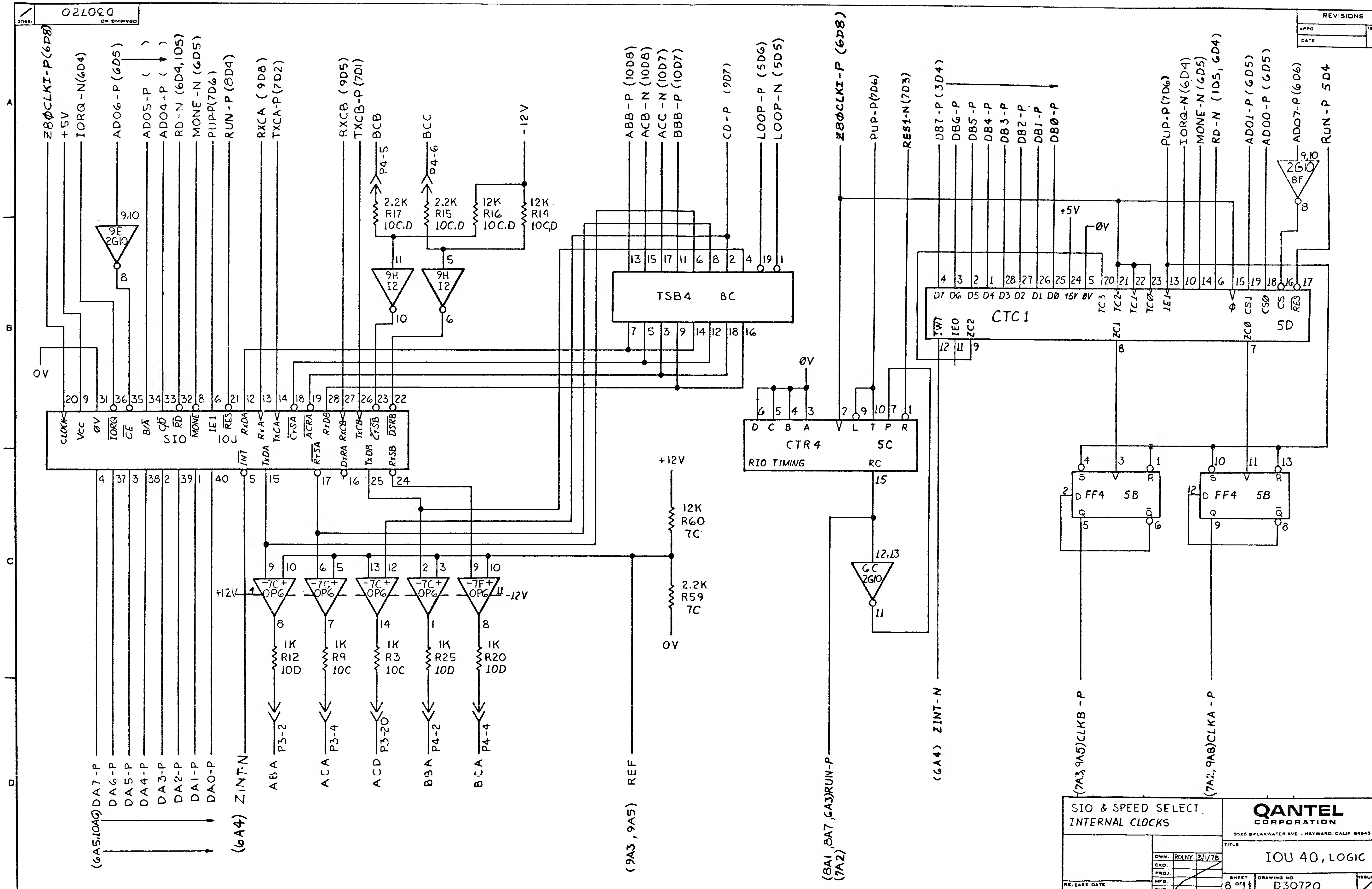

D30720
Z8ØCLKI-P (6D8)
+5V
IORQ-N (6D4)
AD06-P (6D5)
AD05-P
AD04-P
RD-N (6D4, 1D5)
MONE-N (6D5)
PUP-P (7D6)
RUN-P (8D4)
RXCA (9D8)
TXCA-P (7D2)
RXCB (9D5)
TXCB-P (7D1)
BCB
BCC
-12V
P4-5
P4-6
2.2K R17 10C,D
2.2K R15 10C,D
12K R16 10C,D
12K R14 10C,D
9H I2
9E 2G10
ABB-P (10D8)
ACB-N (10D8)
ACC-N (10D7)
BBB-P (10D7)
CD-P (9D7)
LOOP-P (5D6)
LOOP-N (5D5)
TSB4 8C
Z8ØCLKI-P (6D8)
PUP-P (7D6)
RES1-N (7D3)
DB7-P (3D4)
DB6-P
DB5-P
DB4-P
DB3-P
DB2-P
DB1-P
DBØ-P
+5V
ØV
CTC 1 5D
PUP-P (7D6)
IORQ-N (6D4)
MONE-N (6D5)
RD-N (1D5, 6D4)
AD01-P (6D5)
AD00-P (6D5)
AD07-P (6D6)
RUN-P 5D4
2G10 8F
ØV
SIO 10J
CTR4 5C
RIO TIMING
+12V
12K R60 7C
2.2K R59 7C
ØV
7C OP6
7F OP6
+12V
-12V
1K R12 10D
1K R9 10C
1K R3 10C
1K R25 10D
1K R20 10D
6C 2G10
FF4 5B
FF4 5B
P3-2
P3-4
P3-20
P4-2
P4-4
(6A5,10A6) DA7-P
DA6-P
DA5-P
DA4-P
DA3-P
DA2-P
DA1-P
DA0-P
(6A4) ZINT-N
ABA
ACA
ACD
BBA
BCA
(9A3, 9A5) REF
(8A1, 8A7, 6A3) (7A2) RUN-P
(6A4) ZINT-N
(7A3, 9A5) CLKB-P
(7A2, 9A8) CLKA-P
REVISIONS
SIO & SPEED SELECT INTERNAL CLOCKS
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SHEET 8 of 11
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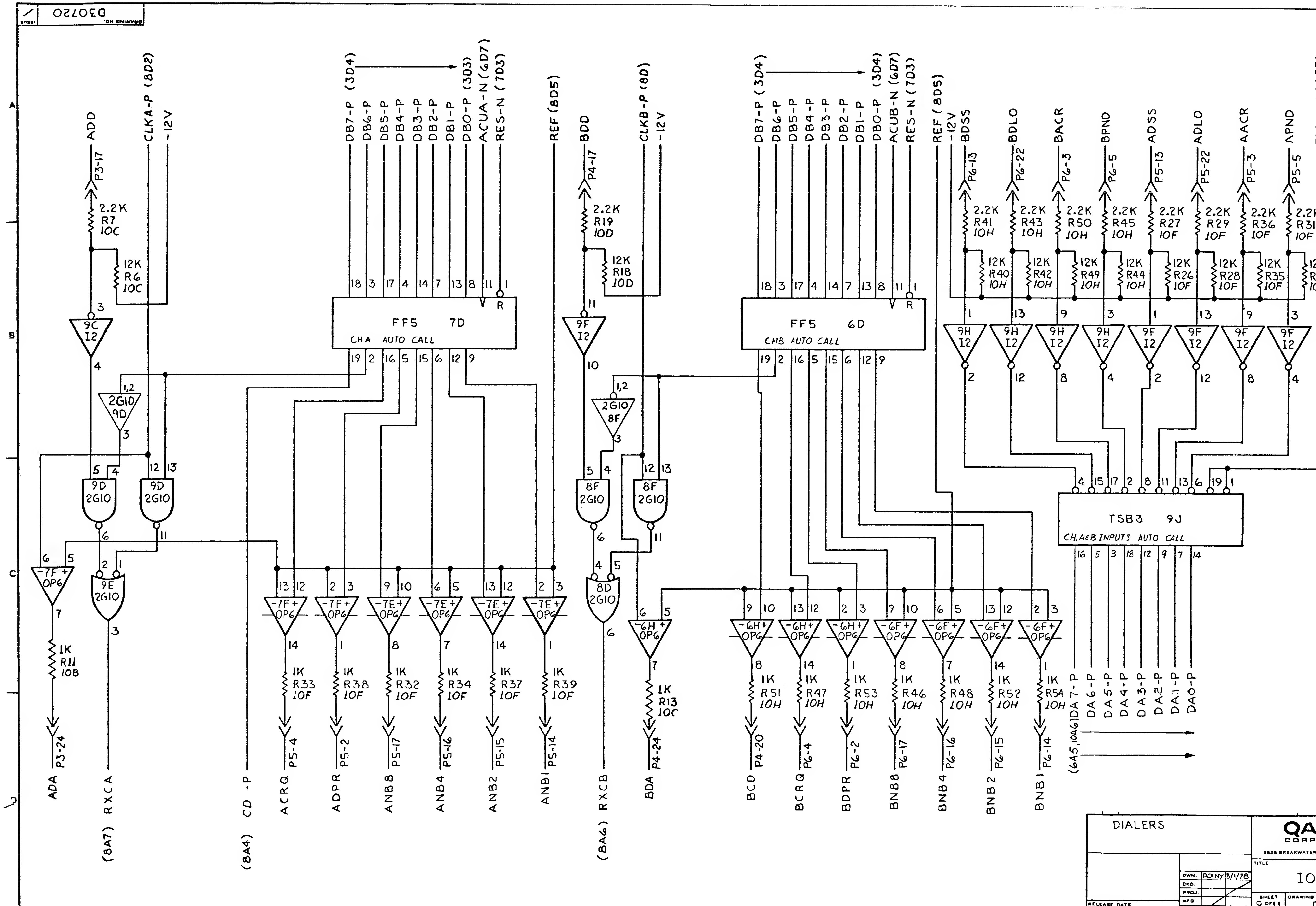

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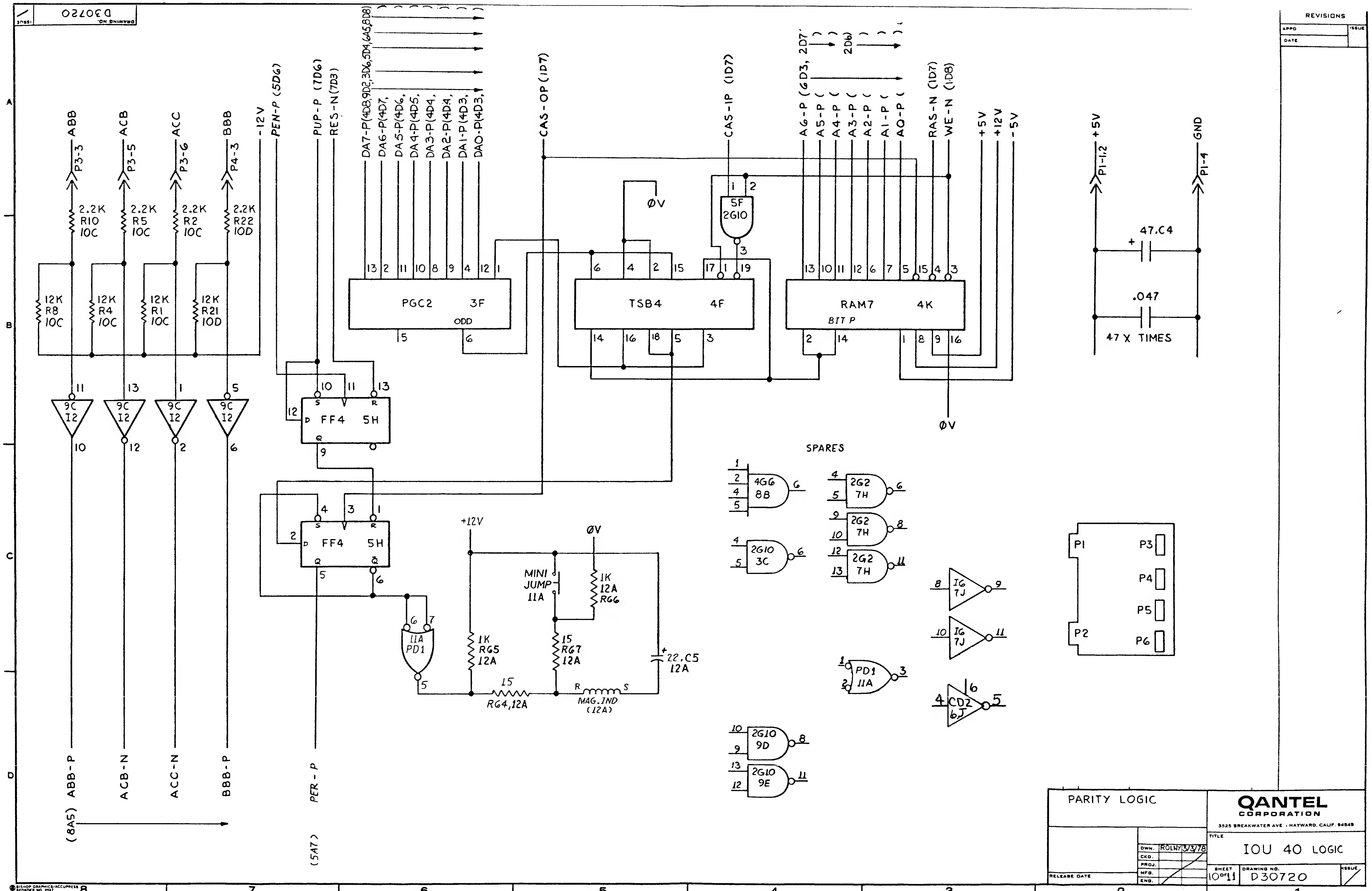

PARITY LOGIC

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SHEET 10 OF 11

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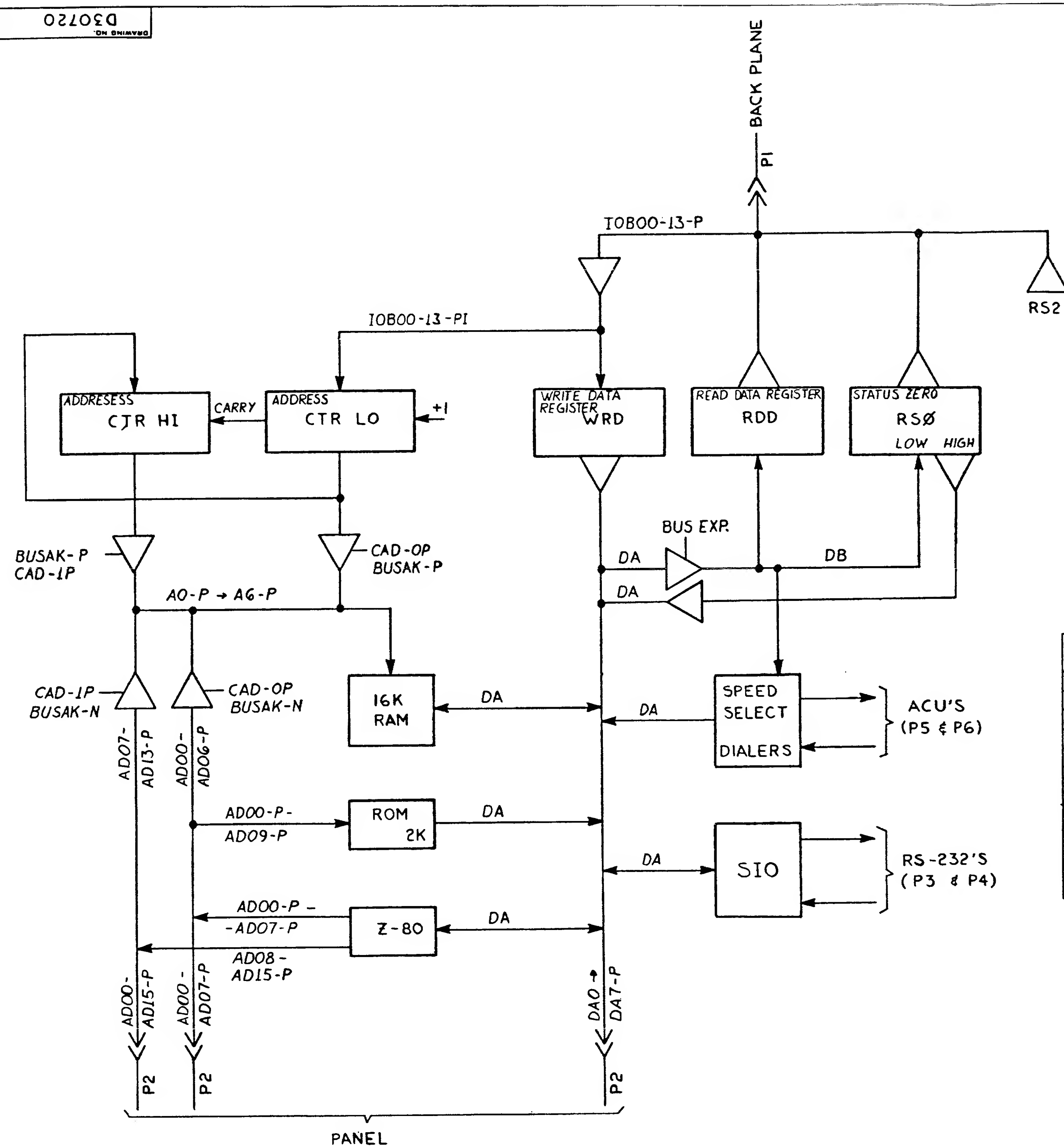

P1: BACKPLANE CONNECTOR 30 PIN 0.156 IN.

1	+5V	+5V	2
3	STROBE-N	GND (ØV)	4
5	+12V	IOEO-N	6
7	IOE1-N	IOE2-N	8
9	IOE3-N	GND (ØV)	10
11	INT-N	GND (ØV)	12
13	IOBOO-P	IOBO1-P	14
15	IOBO2-P	IOBO3-P	16
17	IOB10-P	IOB11-P	18
19	IOB12-P	IOB13-P	20
21	GND (ØV)	GND (ØV)	22
23	GND (ØV)	GND (ØV)	24
25	PFL-N	GND (ØV)	26
27	-12V	SRES-N	28
29	+26V	+26V	30

P2: Z-80 PANEL CONNECTOR 50 PIN 0.1 IN.

1	GND (ØV)	GND (ØV)	2
3	+5V	+5V	4
5	IORQ-N	BUSAK-N	6
7		RD-N	8
9	AD06-P	RES-N	10
11	AD01-P	AD07-P	12
13	AD03-P	AD00-P	14
15	IORD-P	AD05-P	16
17	MREQ-N	WR-N	18
19	MONE-N	AD04-P	20
21	RFSH-N	AD02-P	22
23	IOWR-P	NMI-N	24
25	DA6-P	AD12-P	26
27	DA1-P	AD14-P	28
29	DA0-P	AD08-P	30
31	DA4-P	AD15-PE	32
33	DA5-P	AD09-P	34
35	DA3-P	AD10-P	36
37	DA2-P	AD11-P	38
39	DA7-P	AD13-P	40
41	BUSRQ-N	ZINT-N	42
43	HALT-N	WAIT-N	44
45	Z80CLK-P	FASTCLK-P	46
47	+5V	+5V	48
49	GND (ØV)	GND (ØV)	50

P3 (CHANNEL A) & P4 (CHANNEL B) 25 PIN CONNECTORS

1	CHASSIS STRAP (NOT CONNECTED TO OV)
7	ØV (GND)
2	BA
3	BB
4	CA
5	CB
6	CC
.	.
17	DD
20	CD
15	DB
24	DA

P5 (CH.A) & P6 (CH.B) 25 PIN CONNECTORS

1	CHASSIS STRAP (NOT CONNECTED.)
7	OV (GND)
2	DPR
3	ACR
4	CRQ
5	PND
13	DSS
14	NB1
15	NB2
16	NB4
17	NB8
22	DLO
23	+12V
24	-12V

REVISIONS

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TITLE: LOGIC, IOU 40

DWN. ROCKY 4/7/78
CKD.
PROJ.
MFG.
ENG.

RELEASE DATE

SHEET 11 OF 11 — DRAWING NO. D30720 — ISSUE

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